~~SYSTEM BOARD~~

~~GW BASIC~~

WP 5.0

3M ENHANCED PERFORMANCE DISKETTES

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PREFACE

Congratulations on your purchase of **LCAS©**. This engineering software has been carefully crafted to provide a valuable service not readily available to hardware design engineers before.

You are probably anxious to get started using LCAS, but please don't bypass reading the manual. One main purpose of this manual is to get you started as quickly as possible. Old hands at computer use can first read the Appendix for experienced users, but should still read through the manual to learn LCAS' capabilities and operating procedures. The appendix on "Often Overlooked Features" contains many of the not-so-obvious features that are very useful, but often overlooked.

You will get more out of LCAS now and in the long run by taking the time to read through this manual.

WHAT THIS PACKAGE CONTAINS

Your new Linear Circuit Analysis and Simulation package contains the following items:

1 User's Manual

1 LCAS program diskette

1 LCAS demonstration diskette

The LCAS© program diskette is not copy protected for your convenience. Do not make copies of this manual or the LCAS program except for personal backup use.

The demo diskette may not be sold or altered in any way. However, feel free to reproduce and give copies of the demonstration diskette to your friends and associates.

The User Support Plan (Appendix X) gives full instructions on registration of this program, calling for assistance in operating LCAS and information on future updates.

If you have comments or suggestions on the LCAS program or this manual use the comment form in the rear of this manual or write us a letter. We at DATUM SYSTEMS are always interested in ways of improving our products.

The LCAS© program and this manual are protected by copyright law.

THE LAYOUT OF THIS MANUAL

This manual has five major sections:

1. Getting Started with LCAS -

Includes the introduction, making backup and working copies of LCAS, configuration and a set of tutorial type procedures to familiarize you with the functions and operations in LCAS. Two example working sessions are used to show typical procedures.

2. Detailed Command Reference -

Includes the detailed procedure for operation of each of LCAS' functions and commands. This section is ordered in the general sequence of circuit analysis, from inputting information, editing and manipulating components, analyzing and finally outputting tabular or graphic information.

3. Detailed Component Reference -

Lists each of the component types and variations resident in LCAS. Notes and examples detail component usage.

4. Command/Menu Summary -

Provides a short detail of all commands and key functions.

5. Appendices -

Includes tips and techniques, a mini-tutorial on the use of Phase Locked Loops, file structures, a quick start for experienced users, circuit examples, error messages, etc.

The Index

Options

Space is provided for optional programs and utilities which interface with LCAS.

NOTATION USED IN THIS MANUAL

Several conventions are used to describe common keystroke functions and operations specific to DOS and LCAS.

The keystrokes you press to perform an action are normally shown on a separate line and in bold face type as in -

/FCY

indicating the consecutive keystrokes "/", "F", "C" and "Y".

When movement of a cursor (explained later) to a specific point is required it is shown on the same line as keystroke commands but in braces, as in -

/D {Cursor down to xxxx}

Keystrokes are always shown in uppercase for consistency, but may actually be performed in upper or lower-case. The one exception is the multiplier "M" where a small "**m**" is used to denote milli- and a large "**M**" used to denote Mega- as detailed in Part 2 under component entry.

When pressing the "Return", "Enter" or ↵ key is required, it is shown in text as **[Return]**. Some keyboards name the **[Return]** key as "**Enter**".

Likewise all other named keys, such as "Esc" and "PgUp", are shown in text as **[Esc]** and **[PgUp]**, etc. The function keys are shown in a similar manner as **[F1]**, **[F2]**, . . . **[F10]**.

Menu options from the display screen are shown in an enclosing box as in -

Co-processor	Default drive	Printer	Update	Exit

The menu display also uses bold letters to indicate the highlighting on the screen display.

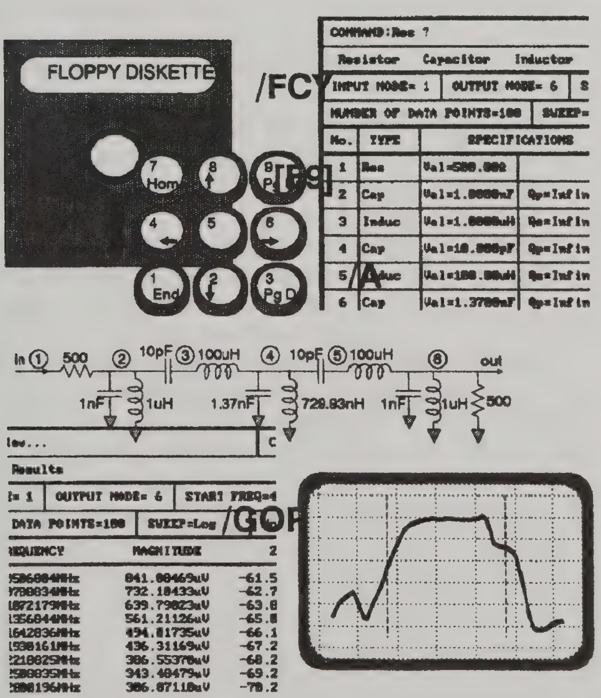
Circuit Schematic Conventions

The schematics throughout this manual use standard schematic conventions. One point worth mentioning is that line crossovers are not shown by a semi-circular crossover, and dots are rarely used to indicate a connection. To differentiate between crossovers and connections:

> connections are shown by a "T" type intersection and
> crossovers are shown as an "X" type intersection.

PART 1 -

GETTING STARTED WITH LCAS


FLOPPY DISKETTE
/FCY
[Pg]
/A
/GOP
COMMAND:Res ?
Resistor Capacitor Inductor
INPUT MODE= 1
OUTPUT MODE= 6
NUMBER OF DATA POINTS=100
No.
TYPE
SPECIFICATIONS
1 Res Val=500.000
2 Cap Val=1.0000nF
3 Induc Val=1.0000uH
4 Cap Val=10.000pF
5 Induc Val=100.00uH
6 Cap Val=1.3700nF
7 Hom
8
9 Pg
4
5
6
1 End
2
3 Pg D
In
500
10pF
100uH
10pF
100uH
out
1nF
1uH
1.37nF
728.83nH
1nF
1uH
500
Results
OUTPUT MODE= 6
START FREQ=
DATA POINTS=100
SWEEP=Log
MAGNITUDE

Introduction

Linear circuit analysis is a powerful tool which enables a circuit designer to prototype, analyze, operate, and compare a circuit to desired performance criteria, all without building the circuit in hardware. LCAS builds a "software prototype" by simulating the circuit's components and interconnections on your personal computer. An engineering analysis is then performed on these simulated components to yield the circuit's magnitude, phase and delay response versus frequency. The analysis results can then be presented graphically and printed out.

One major advantage of a computer simulated circuit is the ease with which the circuit's component values and configuration can be changed to test performance and produce desired results.

Early linear circuit analysis programs were based on only a few very basic components, such as resistors, capacitors, inductors, and voltage controlled current sources. These programs were difficult to use even by experienced engineers because more complex, but commonly used components, such as transistors, op-amps and transmission lines had to be individually built from these more basic parts. The whole process of editing, analyzing and viewing results required multiple programs. Not only was this process tedious and slow, it was error prone. In addition these early programs rarely gave graphical analysis results.

Welcome to LCAS

LCAS goes well beyond previous linear circuit programs in several important respects:

- LCAS pre-defines all the commonly used components within itself.
- LCAS includes a complete integral set of file handling, editing, graphing and printing capabilities which make use of the program natural and easy.
- A complete component editor makes circuit entry and modification easy.
- LCAS includes unique Phase Locked Loop analysis capabilities.
- An integral delay element allows analysis of complex functions such as transversal filters.
- LCAS computes Group Delay and effective Noise Bandwidth.
- LCAS is highly interactive.
- LCAS is extremely fast!

LCAS stands for Linear Circuit Analysis and Simulation. As the name implies it is a program that analyzes and simulates linear circuits. LCAS does not work on circuits which contain non-linear elements. Non-linear elements are circuit components whose output does not follow a linear relationship with its input. Examples of non-linear elements are diodes and all digital switching circuit components.

LCAS includes all the common linear circuit components such as resistors, capacitors and inductors; active transistors and op-amps; and special components like transformers and transmission lines. LCAS also includes many unique elements such as a

VCO, phase detector and divider as integral parts of phase locked loop circuits.

The inclusion of a "delay" in the divider and as an independent element allows a wide variety of complex and realistic simulations. Long feedback loops common in communications systems are easily simulated with delay, as are the varieties of digital filters that are based on delay such as transversal filters.

LCAS does not limit the user to only simplistic component definitions. Many components include special cases and parameter entries that allow you to simulate real world circuits. For instance you have the ability to define tapped inductors and transformers, and add "Q" factor to inductors and capacitors. You can even define the various transmission line elements as either coaxial, microstrip, balanced or even delay lines. Many of these transmission lines are defined by their physical dimensions.

Very large circuits with as many as 128 components and 64 nodes may be analyzed at one time. Circuits may also be analyzed individually and summed serially to yield the net result of the entire combination. Likewise, circuits can be analyzed and subtracted from each other to yield errors or relative differences.

A very fast easy-to-use component editor is also provided to input and change components to any type, value, or configuration desired. Circuits, once created, may be saved to disk and used at any time for later reference. A library of circuits may be created and used as components, by merging those circuits into the circuits you are creating.

Files are easily managed within LCAS. Circuit files created with LCAS can be saved, loaded, merged and erased allowing complete control of disk data. A circuit file directory is also provided, and includes the date and time that the files were created.

LCAS supports both the monochrome and color display adapters. If only a monochrome display adapter is installed, the program will function normally, except that the analysis data can

not be graphed. Therefore, any of the graphic related functions such as group delay, noise power, addition and subtraction are not supported. If only a color graphics display adapter is installed, then all modes of operation are supported. If both types of display adapters are installed, then all modes are supported with the added feature of having continuous graphic information, with menu options displayed while in graphics mode.

LCAS optionally supports the Intel 8087/80287 math co-processor. When installed and configured properly, the 8087 will increase the speed of analysis by approximately nine times on medium-sized circuits. This increase in speed is very significant and is well worth the price for anyone who makes regular use of this program.

LCAS carries out all internal calculations to 16 digit precision and prints out all results to 8 significant digits. The dynamic range is greater than 10 to the plus or minus 47th power (over 750dB) without an 8087 installed. When an 8087 is used the dynamic range is increased to 10 to the plus or minus 493rd power (over 6000dB!).

This manual and the LCAS program assume that the user is familiar with the basics of electronic circuits and design. LCAS can however be an invaluable aid while learning to design electronic circuits, allowing the student to quickly test his ideas and knowledge.

> *Please Take Note:*
>
> *LCAS does not design circuits, nor will it correct a poor circuit design. It is a designer's tool used to simulate and analyze an already existing or new circuit design.*

OPERATIONS OVERVIEW

LCAS presents three display screens in operation:

* **The Component Screen** is the circuit editor display. This screen allows entry and manipulation of the circuit components.

* **The Analysis Results Screen** displays the tabular results of analysis of the circuit present in the editor.

* **The Graphic Screen** displays a graphic representation of the analysis results and allows modification and overlays of graphically presented data.

LCAS is a highly interactive program, allowing you to easily switch between these screens at will, repeatedly editing, analyzing and graphing circuit performance.

Hardware Requirements

The hardware requirements for operation of LCAS are minimal, although added hardware features may make use easier. LCAS requires 640K of random access memory (RAM) and one double sided double density disk drive. The program must operate under PC-DOS™ or MS-DOS™ Version 2.00 or later to function properly.

Computer

LCAS is designed to function normally on any IBM PC, XT or AT and also supports most compatibles. The program requires 640K of RAM. Additional extended or expanded memory installed is not included in the 640K, and is not used by LCAS. Loading of memory resident programs may reduce the amount available to LCAS below its minimum.

If insufficient memory is available, the program will notify you and return to DOS. Even a computer with the required 640K RAM, may require removal of memory resident programs for proper operation of LCAS.

LCAS is designed and intended to operate with an 8087 or 80287 installed. LCAS will operate without a co-processor, but its capabilities are severely limited by the lack of dynamic range during internal calculations.

Display Requirements and Options

A color/graphic display adapter is recommended. LCAS will operate with a monochrome display adapter only, but will not then display magnitude, delay and phase response graphs.

If both monochrome and color/graphics adapters are used, LCAS will recognize and use both; the monochrome for display of circuit elements and analysis results, and the color/graphic for display of magnitude, delay and phase response graphs. Having both adapters also allows display of the graphic screen manipulation menus on the monochrome screen, while maintaining the graphic screen.

An Enhanced Graphics Adapter (EGA) and color or enhanced graphic monitor may be used instead of the color/graphics adapter/monitor. The EGA may not reproduce the normal blue background color used for graphic display of analysis data depending upon the adapter type and emulation mode.

Printer

LCAS does not require a printer to operate, but having one provides valuable hardcopy information. LCAS can use any printer for output of component and tabular analysis information.

Printing of graphic information requires a dot matrix printer adhering to Epson graphics standards and a color/graphic display adapter. Refer to the section on "Outputting Data" for more information on tested printers.

Installation

Before you get started using LCAS there is a minimal amount of installation that must be performed. In this section we will accomplish two things:

1. Make an important backup of your master diskette.
2. Make a working copy of LCAS on either floppy or hard disk for day to day use.

The first step is to protect your master diskette by making a copy and storing the original in a safe place. The LCAS program diskette is not copy protected. The following procedure requires a blank or unused diskette, either formatted or unformatted.

> *CAUTION : any existing information on the diskette chosen to put your LCAS backup on will be overwritten by the following procedure.*

The backup master diskette is created using the DOS "diskcopy" command. This step should be performed whether you have a hard disk or not.

Procedure for ALL users:

1. Start up your computer with the DOS Master Diskette in Drive A, or start from your hard disk in the usual manner. You should now have the familiar DOS "A" (or "C") prompt visible. Hard disk users should go to the directory containing the DOS "DISKCOPY" command file.

2. Issue the DOS command -

```
DISKCOPY   A:  B: [Return]
```

3. When prompted, place your LCAS master diskette in drive A, and a blank diskette in drive B. Follow the DOS prompts to create the new LCAS master copy.

4. Label your new copy "LCAS MASTER BACKUP", and place the original master diskette in a safe place. You will use the newly created backup in making an LCAS working copy. Go to the section titled "Creating an LCAS Working Copy" below.

Creating an LCAS Working Copy

The master of the LCAS program is supplied on a standard diskette without the DOS system installed. The LCAS program is not copy protected for your convenience. To create a working copy of LCAS we will simply place the LCAS program (LCAS.EXE), it's initialization file (LCAS.INT) and several sample files onto a DOS formatted system diskette, or hard disk.

The initialization file, LCAS.INT, is read by LCAS on startup to determine where to look for files, if an 8087 math co-processor is present and if you have defined a set-up string to be sent to a printer and the printer port.

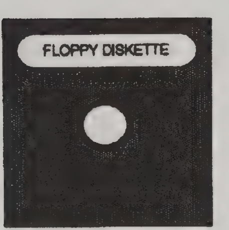
LCAS allows circuit files (these are circuit descriptions which you create and are described later) to be placed on any drive or directory, either with the program, or on a separate diskette.

We know that every new program can be intimidating, especially if your computer is also new. A lot of the initial steps may not make sense, but patiently bear with us for now. Remember that the master copy will allow you to recover gracefully from any mistake.

The working copy of LCAS can either be placed on your hard disk if you have one or on a DOS formatted diskette. To make the creation of a working copy easier, two batch files have been provided on the master diskette for common installations. The

batch file "INSTHARD" will install LCAS on a hard disk and "INSTFLOP" will install LCAS on a floppy diskette.

Figure 1-1 shows the disk configurations represented by these installation options.



DOS System Diskette contains:

COMMAND.COM
LCAS.EXE
LCAS.INT
CIRCUIT FILE 1.LCA
CIRCUIT FILE 2.LCA
.
.

Installation Type A. On Floppy Diskette

Hard Disk contains:

**Root Directory **
COMMAND.COM
LCAS.BAT
.
.
\DATUM Directory
LCAS.EXE
LCAS.INT
\LCAS Directory
CIRCUIT FILE 1.LCA
CIRCUIT FILE 2.LCA
....

Installation Type B. On Hard Disk

Figure 1-1 Installation Options

Option A. Installation on a Floppy Diskette

Installation on a floppy diskette requires one formatted DOS diskette with the system installed. If you are not familiar with the procedure for creating a DOS system diskette then refer to your DOS manual for the proper method. The normal method for creating this system diskette is to place the DOS Master diskette in drive A, make drive A the default drive and issue the DOS command -

```
FORMAT B:/S   [Return]
```

and follow the DOS prompts.

The procedure below will place the LCAS program and the sample circuit files on the DOS system diskette described above. In order to fit the LCAS working program and circuit files, this diskette should not have other files on it. Additional circuit files may be kept on other diskettes.

Computers with a single or dual disk drive use the same procedure.

1. Place the LCAS Master copy diskette in the A Drive.

2. Make drive A the default by issuing the DOS command -

   ```
   A:   [Return]
   ```

3. Invoke the batch file by issuing the command -

   ```
   INSTFLOP   [Return]
   ```

The INSTFLOP program will have you place the newly formatted diskette in the B: drive. Any errors in completing the installation will be reported.

Option B. Installation on a Hard Disk Drive

The LCAS program and circuit files will be installed on your hard disk drive. This command will create a new directory on your hard disk immediately under the "root" directory with the name "DATUM" and then place the LCAS program in that directory. Sample files will be placed in a directory under the DATUM directory named "LCAS".

1. Select the hard disk as the default drive. If you have more than one hard disk, select the one you wish to place LCAS on as the default.

C: [Return] (or D: if applicable.)

2. Place the LCAS Master copy diskette in the A drive.

3. Then invoke the batch file with the command -

A:INSTHARD [Return]

Note: The "INSTHARD" batch file will not alter any existing files on your hard disk. It will place a startup batch file, named LCAS.BAT, in the root directory. If you maintain batch files in a separate directory, copy this file to your batch directory and delete the root directory file.

For All Users

Other alternative installations are possible, based on the user's requirements. Basically, LCAS can be placed on any disk with sufficient space and its circuit files located anywhere accessible by DOS. Experienced users should refer to Appendix G for more information.

You now have a working copy of your LCAS diskette. The configuration of your new LCAS working copy for your computer hardware is accomplished in the next section during familiarization. The default configuration used by LCAS as shipped (or when no LCAS.INT file is found) will allow startup on any computer hardware setup.

Special Installation Option for Epson FX Printers

For users with the Epson "FX" type printers that accept the Epson format of downloadable fonts, a special file is included on the master program disk. This file is named FX-EPSON.INT and replaces the standard LCAS.INT file. It includes a printer setup string containing the downloadable font set to emulate the IBM character set.

To use this file, you will replace the LCAS.INT file placed on the working floppy diskette or in the \DATUM directory of your hard disk.

Place the backup copy of the master diskette in the **A:** drive. If your working program is on a floppy diskette place it in drive **B:**.

Issue the following DOS command for the installation type-

```
COPY   A:FX-EPSON.INT  B:LCAS.INT
```

for a floppy installation, or

```
COPY   A:FX-EPSON.INT  C:\DATUM\LCAS.INT
```

for a hard disk installation. Use the **D:** drive designator if required.

When LCAS prints to a printer it precedes the text with the downloaded font.

Caveats

DATUM Systems has made every effort to make the LCAS program error free and tolerant to hardware and user errors. The PC and its' clones however are not perfect. Especially computers with several hardware enhancements and memory resident programs are subject to catastrophic failures. These failures may be parity errors, or "lock-up" where the computer becomes totally non-responsive to user input. Usually the only method of recovery from these situations is to turn off the computer, wait a few minutes and restart.

There are two known cases which cannot be trapped within LCAS that result in some form of computer lock-up or loss of resident information.

1. Pressing the key combination **Alt-Ctrl-Del**. This will perform a re-boot of the computer, and is built into DOS by design.
2. Pressing the key combination **Alt-Ctrl-Break**. This may lock-up the computer.

The best prevention to accidentally losing data is to save your circuit files on a regular basis. Then even if the power goes off, you are protected as of your last save.

First Encounter

Starting the LCAS program is very easy. The following steps are used to run LCAS -

Floppy Disk Users:

1. Place the working copy diskette in drive A. (You may run LCAS from any drive, simply replace the drive designator "A" with the desired drive.)

2. Make drive A the default by issuing the DOS command-

```
A:  [Return]
```

3. Start LCAS by issuing the command -

```
LCAS  [Return]
```

LCAS will now load and display the title screen.

> *NOTE: For single drive users. After pressing any key as requested by the title screen, you may remove the LCAS Program diskette and place the diskette with your circuit files in drive A.*

Hard Disk Users:

If you have installed LCAS on your hard disk using the "INSTHARD" installation file then a batch file named LCAS.BAT was placed in your root directory which will invoke LCAS. Simply issue the command -

```
LCAS  [Return]
```

If the "LCAS.BAT" batch file has been removed then you must first change to the \DATUM directory by issuing the DOS command -

```
CD  \DATUM  [Return]
```

Note that the symbol preceding DATUM is a BACK-slash.

Then invoke the LCAS program with the command -

```
LCAS  [Return]
```

The above two commands are actually the contents of the LCAS.BAT batch file.

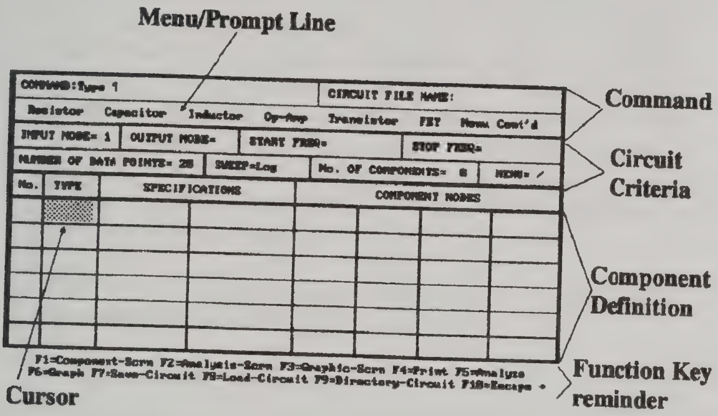
LCAS will now load and display the title screen.

The Display Screens

Pressing any key will remove the Title and copyright notice, and display the main default screen.

LCAS is now completely resident in memory. Once the program is started the program diskette need not be kept in drive A (or the drive LCAS was started from).

Look over this screen now. It is called the "Component Screen", and is used for displaying and editing the components in the circuit to be analyzed. Figure 1-2 is a view of the component screen at startup. We will later describe how to view two other information screens in LCAS.



```
COMMAND:Type 1                              CIRCUIT FILE NAME:
Resistor  Capacitor  Inductor  Op-Amp  Transistor  FET  Menu Cont'd
INPUT NODE= 1   OUTPUT NODE=   START FREQ=            STOP FREQ=
NUMBER OF DATA POINTS= 25   SWEEP=Log   No. OF COMPONENTS= 0   MENU= /
No.  TYPE       SPECIFICATIONS              COMPONENT NODES
F1=Component-Scrn F2=Analysis-Scrn F3=Graphic-Scrn F4=Print F5=Analyze
F6=Graph F7=Save-Circuit F8=Load-Circuit F9=Directory-Circuit F10=Escape +
```

Figure 1-2 Main Component Screen

The component screen is divided into four sections:

1. The command section in the top two lines of the screen,
2. The circuit criteria section in the next two lines,
3. The component definition section in the lower portion of the screen, and
4. The last two lines of the screen contain function key reminders.

In the command section, the very upper left of the screen is the "Command" cell. This cell contains a prompt and a small underline blinking cursor.

To the right of the Command cell is the "Circuit Name" cell which displays the name of the circuit being analyzed. This cell will remain blank until a circuit is named.

Below these two cells is the menu/prompt line, which displays the list of possible choices at each level of a command. In the

default condition this line displays the list of possible components which may be selected. Note that the first letter of each component name is highlighted on the display. If it's not highlighted then your contrast and brightness controls require adjustment. The highlighting is intended to show the proper key to press to select each of the components. For instance, the first "R" in "Resistor" is highlighted, indicating that the resistor is selected by pressing the "R" key. Note that selecting any item from the menu/prompt line does not require pressing the **[Return]** key afterward.

The circuit criteria section contains cells to define the parameters for analyzing the present circuit.

The component definition section contains a large inverse cursor in the first "TYPE" cell. LCAS keeps track of the component number in the leftmost cell labeled "No.". The inverse cursor shows the location of the active entry.

The function key reminders on the last two lines of the screen show the function keys used as quick replacements of common multi-key functions.

Two other "screens" are also available, but only after a circuit analysis has been performed. The "Analysis" screen can be selected by using the **[F2]** function key, while the **[F1]** returns to the component screen. The analysis screen is also automatically selected if an analysis is performed (more on this later). The third screen is the graphic screen which is displayed on a color graphic/monitor only. The graphic screen will not be displayed unless an analysis has been performed and the results graphed.

Issuing Commands

LCAS is both a command driven and a menu driven program. The structure of issuing commands to LCAS is similar to that of typical spreadsheet programs like Lotus $1^2 3$. A large inverse cursor is used to indicate your present cell position and where input information will be placed. There is also a small blinking

underline cursor and question mark in the command cell, whenever LCAS is awaiting an input. Command inputs can be of three types at this point:

1. A highlighted letter selecting one of the options in the menu/prompt line or,

2. A function key selecting one of the options on the lower function key reminder lines or,

3. Striking the slash character, "/" which brings up a new command menu in the menu/prompt line.

   Note that the 4th line of the screen reminds you of this command with "**MENU** = /". The rest of this manual will refer to commands beginning with the slash character as "slash" commands.

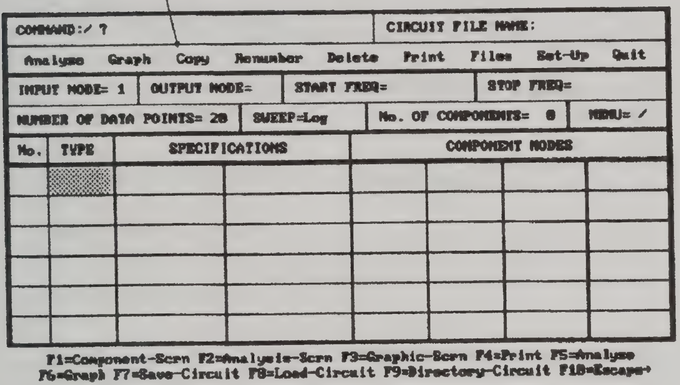
The blinking underline should be in the command cell now. Press the slash "/" key and the prompt line will change to show next level of possible commands. These are:

Analyze **G**raph **C**opy **R**enumber **D**elete **P**rint **F**iles **S**et-up **Q**uit

Figure 1-3 shows the changed prompt line in this command mode.

Notice again that in our text and also on your screen the first letters of the words on the Menu/Prompt line are displayed in bold indicating the key to press for that option.

Next press the "S" key to call "Set-up" and a new level of commands becomes visible on the prompt line. Press the **[Esc]** ("Escape") key and the command level will pop back one level. This is the standard procedure throughout all of the LCAS commands and functions; each new key press takes you to a new command level and each press of **[Esc]** backs out of the last command level or "escapes".



First letter of each option Bold

```
COMMAND:/ ?                                CIRCUIT FILE NAME:
 Analyse  Graph  Copy  Renumber  Delete  Print  Files  Set-Up  Quit
INPUT NODE= 1 | OUTPUT NODE= | START FREQ=          | STOP FREQ=
NUMBER OF DATA POINTS= 20 | SWEEP=Log | No. OF COMPONENTS=  0 | MENU= /
No. | TYPE |      SPECIFICATIONS      |       COMPONENT NODES
F1=Component-Scrn F2=Analysis-Scrn F3=Graphic-Scrn F4=Print F5=Analyse
F6=Graph F7=Save-Circuit F8=Load-Circuit F9=Directory-Circuit F10=Escape→
```

Figure 1-3 "Slash" Command Prompt

The [F10] is a quick way to abort any pending command and return to the main command level.

Quitting LCAS

Quitting LCAS returns to the DOS operating system. To quit LCAS use the slash command -

```
\QY
```

representing the quit command followed by the response "Y" to the prompt "Exit (Y/N)?"

The version number and serial number of your copy of LCAS is shown on the menu/prompt line with the prompt to confirm your desire to quit.

Configuring LCAS

Let's use what we know now to configure LCAS for your particular computer.

press **[F10]** to return to the main command level.

press "/" for commands.

press "S" for set-up.

You are now presented with 5 choices in the prompt line shown below. These are:

```
Co-processor  Default drive  Printer  Update  Exit
```

Select each of these in turn to configure LCAS for your computer setup. Some notes are given for each of these items below:

Co-processor - If you have an 8087 (or 80287/387) Numeric Data Processor installed then press **"Y"** for yes. If you do not have an 8087, then press **"N"** for no. By just pressing the **[Return]** key you retain the previous setting.

Do not answer yes if you don't have an 8087.

LCAS will allow you to force the setup to indicate an 8087 even if one is not found in the computer. When you attempt to run the analysis portion of the program this way, LCAS will override your configuration. This is necessary because programs attempting to use a non-existent 8087 usually "lock-up", resulting in the loss of any information in memory.

LCAS will check to see if an 8087 is present when the configuration option is set to "Yes", and warns you if one is not found. This facility can be of use if you are not sure whether the com-

puter you are using has an 8087 installed. Simply select the "Yes" response to the co-processor setup prompt and the lack of a warning indicates the presence of an 8087. If one is not found you should reset the option to "No".

The computer's hardware switch setting for the 8087 does not affect this entry.

Default drive - LCAS allows you to set four different drive and paths to use as the default in loading and saving files, and in performing directory displays; one each for Circuit, Text, Data and FFT Files.

When you select the Default Drive option you are presented with another menu allowing you to select which of these to set.

Circuit Files   Text Files   Data Files   FFT Files

The hard disk installation program will have already set all the files paths to the "LCAS" subdirectory (unless the FX-EPSON.INT file was used which contains no paths). The floppy installation defaults these settings to "none" which chooses the current drive and path. If you have any definite plans for a file structure in mind then set these entries to the drive letter/path desired, otherwise they may be best left unchanged for now. They can always be reset later as you gain more experience with LCAS. Hard disk or floppy users who want to keep files on floppies might want to set the Circuit files entry to **A:** or **B:**.

Path commands may be used and are recommended for keeping files on a hard disk. To keep files in a directory separate from the LCAS program, insert the drive and full path description. To keep files in a directory under the LCAS program, DOS only requires the path from the current directory to the desired directory be specified. For instance, the path "**\DATUM\LCAS**" is the location for files set up by the "INSTHARD.BAT" installation batch file provided with the LCAS program. Refer to the DOS manual for more information on paths and directories.

If you have installed the LCAS program on a hard disk and replaced the LCAS.INT file created by the INSTHARD program with the FX-EPSON.INT file, then you should now set all the file directories to "\DATUM\LCAS".

Legal DOS drive and path names should be used. If only a drive letter (with no subdirectory path) is used then the colon should be used after the drive designation. For example use "**A:**", not just "**A**" to designate the A drive.

Entering a space and **[Return]** designates the current drive and path set as default in DOS before starting the LCAS program. On requesting a directory of files in LCAS this option is shown as a question mark on the file directory heading.

> *NOTE: The Default Drive setting can be over-ridden during a request to load or save a file by preceding the file name with a drive letter and colon; for example "B:CIRCUIT1". Path names may not be used in this method.*

Printer - When you select "**Printer**" from the configuration command menu you are presented with a new menu offering the choice of -

Set-Up String	Printer Port

Set-Up String.

If your printer requires a set-up string to operate, or you wish to place the printer in a special mode then select the Set-Up String option by the command -

S

The ascii decimal number of the Set-Up String's characters can then be entered here with the backslash as the character separator, including the first character. For example to set an

Epson printer to emphasized mode the entry would be "\27\69\". Refer to your printer manual for other codes.

You can enter a sequence of ascii codes until you fill the command entry cell. Then LCAS will beep to inform you that there is no more room. To enter strings longer than will fit in the command cell, first enter codes until the cell is full and press **[Return]**. Then begin a new string but enter a plus (+) and backslash before continuing with more codes. This method can be used successively to enter up to a total of 270 codes.

Users with Epson "FX" type printers should have already converted the special FX-EPSON.INT file for use as described in the Installation section.

Pressing **[Return]** will accept the present set-up string shown and return to the configuration menu.

Printer Port.

Printers can be placed on LPT1:, LPT2:, or LPT3:. To set the port enter -

```
P
```

from the printer menu. The port number is selected by pressing either 1, 2 or 3. Selecting a port number or pressing **[Return]** to accept the existing port designation returns you to the configuration menu.

If your printer is on a serial port, then use the DOS "MODE" command (outside of LCAS) to configure the port for the proper baud rate to match the printer, and assign the "COM" port to LPT1:. For example, the normal method of connecting to a serial printer on serial port 1, operating at 1200 baud might be -

```
MODE  COM1: 1200,N,8,1,P

MODE  LPT1:=COM1
```

Refer to your DOS and printer manuals for the proper form of these commands to use for your equipment. Placing these commands in an "AUTOEXEC.BAT" batch file is usually the easiest way to configure your printer each time the computer is started. The particular commands shown would require that the MODE.COM file be placed on the working diskette in floppy based systems.

Update - selecting this option stores the presently set configuration as the default configuration to a file named "LCAS.INT". LCAS reads this file on startup to determine your default configuration.

> *NOTE ! If the file "LCAS.INT" is removed from the working disk or not found at startup, the program will beep and create a new configuration file with defaults. If this occurs you should reset the startup defaults and update the configuration as explained.*

Exit - this option returns to the main LCAS command level. Any set-up configuration options changed remain effective only for the present session and are lost when LCAS is quit. If the Update option was selected before exiting the set-up menu, the revised configuration is saved to the "LCAS.INT" file for use the next time LCAS is started.

> *NOTE ! If you do not select the update option after changing any of the set-up options, exiting this menu will make the changes valid only for the present session. These changes will be lost when LCAS is quit.*

Now you are ready to begin working with LCAS.

Example Session One -

Basic Operations

To familiarize you with the features of LCAS, following are several sample sessions which allow you to operate LCAS in a realistic analysis of sample circuits. The operating procedures are explained in detail for each step along the way using screen and graph images.

Several sample circuit files have been placed on the working diskette for use in these examples and your study later. We will load one of these files now to get some hands on experience operating and maneuvering within LCAS.

In this first example session we will learn to:

- Get a directory of circuits on disk.
- Load circuit files.
- Control the cursor.
- Analyze circuits.
- Graph analysis results.
- Change component values.
- Overlay graphs.
- Perform an expanded analysis.
- Set graph scales manually.

Loading a Circuit File

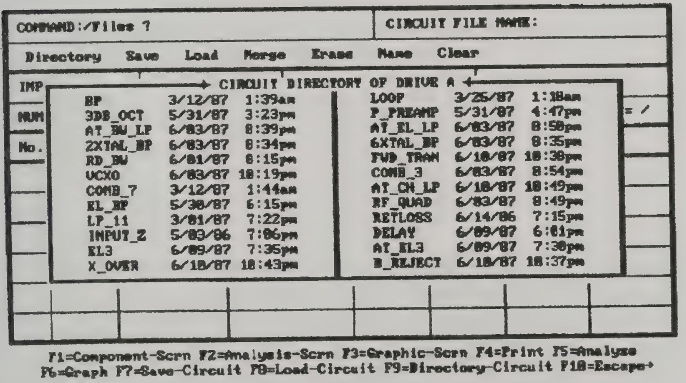
Place the LCAS working copy program diskette in the default drive, as it contains the example circuit files you will be using in this session.

If you have left LCAS since setting up the configuration options, restart the program with the DOS command -

LCAS

Begin a command by first striking the slash key "/". The prompt line will change to that shown in Figure 1-3. Select the "Files" command by striking the "F" key, and on the new prompt the "D" key for "Directory". The complete command used to get a circuit directory in our standard format is -

/FD



```
COMMAND:/Files ?                         CIRCUIT FILE NAME:

Directory   Save   Load   Merge   Erase   Name   Clear

                  CIRCUIT DIRECTORY OF DRIVE A
     BP          3/12/87   1:39am     LOOP        3/25/87   1:10am
     3DB_OCT     5/31/87   3:23pm     P_PREAMP    5/31/87   4:47pm
     AT_BW_LP    6/03/87   8:39pm     AT_EL_LP    6/03/87   8:50pm
     2XTAL_BP    6/03/87   8:34pm     6XTAL_BP    6/03/87   8:35pm
     RD_BW       6/01/87   8:15pm     FWD_TRAN    6/10/87  10:30pm
     VCXO        6/03/87  10:19pm     COMB_3      6/03/87   8:54pm
     COMB_7      3/12/87   1:44am     AT_CH_LP    6/10/87  10:49pm
     EL_BP       5/30/87   6:15pm     RF_QUAD     6/03/87   8:49pm
     LP_11       3/01/87   7:22pm     RETLOSS     6/14/86   7:15pm
     INPUT_Z     5/03/86   7:06pm     DELAY       6/09/87   6:01pm
     EL3         6/09/87   7:35pm     AT_EL3      6/09/87   7:30pm
     X_OVER      6/10/87  10:43pm     B_REJECT    6/10/87  10:37pm

F1=Component-Scrn F2=Analysis-Scrn F3=Graphic-Scrn F4=Print F5=Analyze
F6=Graph F7=Save-Circuit F8=Load-Circuit F9=Directory-Circuit F10=Escape→
```

Figure 1-4
Typical Circuit Directory

A list of the circuit files on disk will then be displayed. A sample directory is shown in Figure 1-4. If no files are found, check that the disk and drive are correct for the location of the circuit files. If you are still experiencing difficulty getting a circuit directory, check back on the setup of "Default Drive" section in "Configuring LCAS".

After performing a directory listing LCAS will return to the "Files" command state, allowing further operations with the directory listing visible. The menu presented at this point is -

```
Directory Save Load Merge Erase Name Clear <Files Contin'd>
```

The last entry "Files Continued" is only present if there are more files on the disk than will fit on the screen. LCAS will wait for one of the highlighted keys to be pressed, or **[Esc]**, **[F10]** or the space bar to abort the function and clear the screen. Pressing the "F" key will display additional files. The presently displayed circuit file list is held when any of the other highlighted keys is pressed. The "D" key will restart the directory listing and is also useful for exchanging the diskette when looking for a file.

Note the names of the files available. One of them is "BP" and others include "LOOP" and "X_OVER"

Load the "**BP**" file (BP is short for BandPass) by consecutively striking the keys -

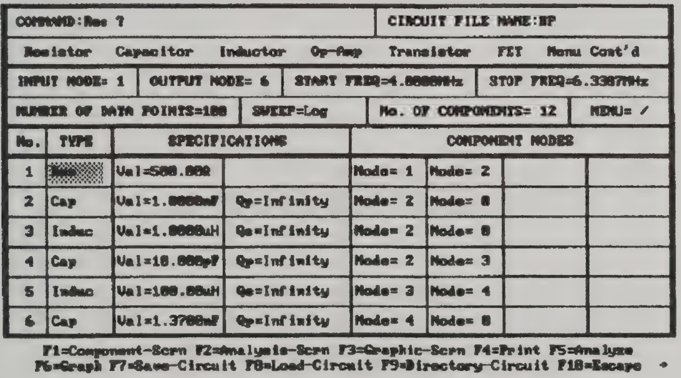
LBP [Return]

For commands and file names, LCAS does not require the use of upper case keys. The "**L**" is for load and the "**BP**" is the file name. The BP file will load very quickly and the component locations at the lower portion of the screen will now be filled. Your component screen should now look like Figure 1-5.

If "BP" did not load correctly, you should have gotten a beep and one of two error messages:

DISK NOT READY !!! or FILE NOT FOUND !!!

Check the drive and make sure the proper disk is loaded and the drive door closed. Look again at the circuit directory and make sure the "BP" file is there.



```
COMMAND:Res ?                                 CIRCUIT FILE NAME:BP
Resistor  Capacitor  Inductor  Op-Amp  Transistor  FET  Menu Cont'd
INPUT NODE= 1  OUTPUT NODE= 6  START FREQ=4.0000MHz  STOP FREQ=6.3387MHz
NUMBER OF DATA POINTS=100  SWEEP=Log  No. OF COMPONENTS= 12  MENU= /
No.  TYPE   SPECIFICATIONS                   COMPONENT NODES
 1   Res    Val=500.00Ω                      Node= 1   Node= 2
 2   Cap    Val=1.0000nF   Qp=Infinity       Node= 2   Node= 0
 3   Induc  Val=1.0000uH   Qs=Infinity       Node= 2   Node= 0
 4   Cap    Val=10.000pF   Qp=Infinity       Node= 2   Node= 3
 5   Induc  Val=100.00uH   Qs=Infinity       Node= 3   Node= 4
 6   Cap    Val=1.3700nF   Qp=Infinity       Node= 4   Node= 0
F1=Component-Scrn F2=Analysis-Scrn F3=Graphic-Scrn F4=Print F5=Analyze
F6=Graph F7=Save-Circuit F8=Load-Circuit F9=Directory-Circuit F10=Escape
```

Figure 1-5 BP Components Loaded

Before proceeding let's try another method of loading a circuit file that is usually easier.

As shown by the reminders at the bottom of the screen, the [F9] function key will perform a disk directory. Press the [F9] key now and the directory will be displayed. Continue the listing if necessary until the desired file name is displayed and then press the "L" key to Load a circuit file. Note that the first file listed in the directory is highlighted by the cursor. Use the cursor (arrow) keys to move the highlight cursor to the BP circuit file,

and press the **[Return]** key. Voila! The BP circuit file is loaded. Using this method you never have to remember or type the name of any circuit file saved to disk.

The schematic of the BP example circuit is given below for reference. The circuit is a bandpass filter centered at 5 MHz. A description of the method of entering circuit information into LCAS circuit files will be given later. First are examples of using the BP circuit file to show basic features and capabilities of LCAS.

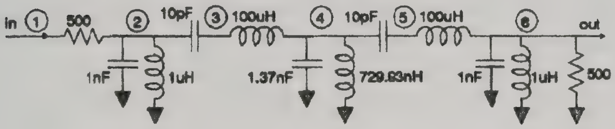


Figure 1-6
Schematic of the BP Example Circuit

The numbers in small circles on the BP schematic are the node numbers, which will be discussed later. The small shaded triangles indicate common or ground connections at node 0.

In the next sections we will first learn to maneuver around the component screen and then analyze and change the circuit.

Cursor Control

Numeric and textual information is placed in "cells" on the component and analysis display screens. The "cursor" control keys are used to move an indicator called the cursor from one cell to another within a text screen. The present location of the cursor indicates where input from the keyboard will be put.

While actually typing at the keyboard the characters and numbers are placed in the command cell, and when the **[Return]** key is pressed this information is transferred to the cell where the cursor is located. This function is similar to the use of the cursor keys within a typical spreadsheet program.

When the graphics screen is present the cursor keys are used to manipulate another form of cursor, appearing as two line markers on the screen.

The cursor control keys are located on the right side of the keyboard as part of the numeric keypad on most keyboards. Some newer keyboards contain a separate cursor keypad on the right. In either case the cursor control keys are depicted by four arrows indicating the direction the cursor will move when pressed.

> If the cursor keys do not give the expected action, make sure that the **[Num Lock]** key (Number lock, toggle key) has not been accidentally set to output numbers. If so press the **[Num Lock]** key once and continue.

First use the right arrow key (→) and watch the cursor move from cell to cell. At the end of a line the cursor will jump to the beginning of the next line. When the cursor reaches the bottom of the screen, the lower portion of the component screen will scroll up to display the remainder of the components. Now use the left arrow key (←) (not the backspace!) and note the reverse action to that of the right arrow.

Continuing to use the left arrow key will take the large inverse cursor into the circuit criteria area.

The up and down arrow keys perform similar functions, so experiment with them now until you feel comfortable with their use. Do not be afraid of harming either the LCAS program or a component file loaded, as no combination of cursor keys can destroy either.

Next try the **[PgUp]** (Page Up) and the **[PgDn]** (Page Down) keys. These will move through the component list a page at a time.

The **[Home]** and **[End]** keys will move to the beginning and end of the component list. When at the beginning of the component listing, pressing the **[Home]** key again will "home" in the circuit criteria area. The **[End]** key has the reverse effect. If already at the home or end position of either area, and the key is pressed again, the cursor will move to the home or end of the other area.

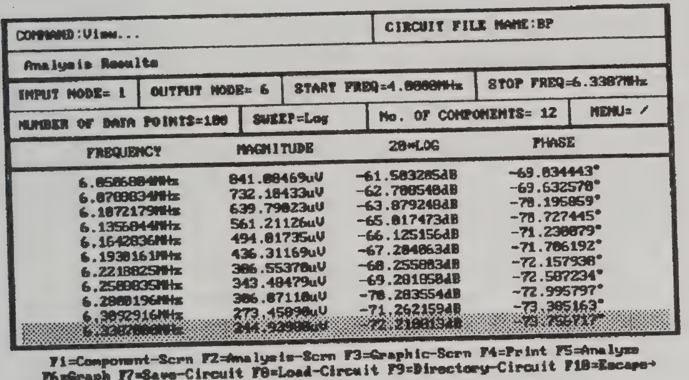
Analyzing the Sample Circuit

Beginning the analysis of a circuit in LCAS is very simple. First note that in the circuit criteria section of the screen including the start frequency, stop frequency, number of data points and whether to step the data points in linear or logarithmic increments are already defined. This is because the last information available is stored with the circuit file when saved. The circuit criteria section must be completed before an analysis can be accomplished on a circuit.

Press the **[F5]** function key and the analysis will begin. Notice that the analysis process is very fast. The analysis routines in LCAS are all written in assembly language for maximum speed and resolution. If you have an 8087 or 80287 Numeric Data Processor installed, and configured LCAS to recognize it, then the analysis is occurring even quicker, probably faster than the screen printing process. The addition of the 8087 co-processor also insures maximum data accuracy due to its internal 80 bit representation of numeric values.

LCAS automatically switched to the second or analysis screen to display the results after the analysis was requested. Figure 1-7 shows the analysis screen after completion of the analysis. LCAS will always switch screens to show requested data.

Pressing any key during the analysis process will abort the analysis. If you accidentally press a key, simply use the **[F5]** function key to redo the analysis.



```
COMMAND:View...                                  CIRCUIT FILE NAME:BP
Analysis Results
INPUT NODE= 1   OUTPUT NODE= 6   START FREQ=4.0000MHz   STOP FREQ=6.3387MHz
NUMBER OF DATA POINTS=100   SWEEP=Log   No. OF COMPONENTS= 12   MENU= /
      FREQUENCY         MAGNITUDE        20*LOG          PHASE
    6.0506804MHz     841.00469uV    -61.503205dB    -69.034443°
    6.0788834MHz     732.18433uV    -62.708540dB    -69.632570°
    6.1072179MHz     639.79823uV    -63.879248dB    -70.195859°
    6.1356844MHz     561.21126uV    -65.017473dB    -70.727445°
    6.1642836MHz     494.01735uV    -66.125156dB    -71.230079°
    6.1930161MHz     436.31169uV    -67.204063dB    -71.706192°
    6.2218825MHz     386.55370uV    -68.255803dB    -72.157938°
    6.2508835MHz     343.40479uV    -69.281850dB    -72.587234°
    6.2800196MHz     306.07110uV    -70.283554dB    -72.995797°
    6.3092916MHz     273.45090uV    -71.262159dB    -73.385163°
    6.3387000MHz     244.92900uV    -72.210013dB    -73.756717°
F1=Component-Scrn F2=Analysis-Scrn F3=Graphic-Scrn F4=Print F5=Analyze
F6=Graph F7=Save-Circuit F8=Load-Circuit F9=Directory-Circuit F10=Escape→
```

Figure 1-7 Analysis Screen

Take a minute to look over the results and try your cursor keys to move through the analysis listing. The cursor control keys now move a full line inverse cursor that allows you to pinpoint any single line in the analysis results. **[Home]** and **[End]** will move to the beginning and end of the results listing. Now press the **[F1]** function key. LCAS switches back to the component screen. Press the **[F2]** function key and LCAS will quickly return to the analysis results.

The top portion of the Component and Analysis screens are the same. You may fill in sections of the Circuit Criteria area from either of these screens.

Graphing the Sample Analysis Results

Now that analysis results data are available, those results can be graphed. Press the **[F6]** function key. If you have a color/graphic or EGA adapter, LCAS will switch to the third or graphic screen, and produce a graph of the data in the analysis screen as shown in Figure 1-8.

If you have both a monochrome and color/graphic screen then both will now contain information. If you have only a monochrome screen then the message **"NO GRAPHICS ADAPTER!!!"** will be displayed in the menu/prompt line of your analysis screen. If you receive this message then you do not have a graphics adapter that LCAS can use. You should then skip over the following section on graphing and instead proceed to "Changing the Circuit".

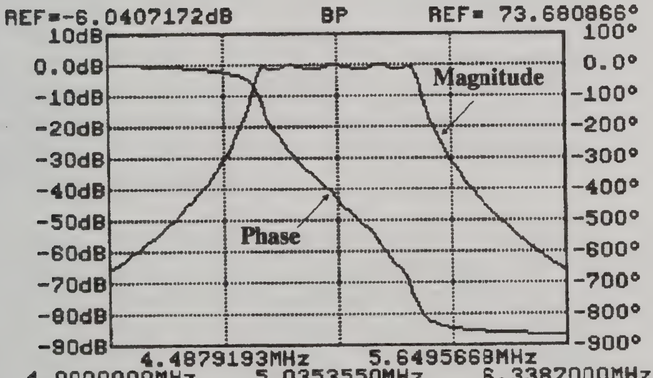


Figure 1-8 Graph of the BP Circuit

Two functions are shown on the graph. Amplitude vs. Frequency and Phase angle vs. Frequency. The magnitude response is normally shown in white and the corresponding magnitude scale on the left of the graph is also shown in white. The magenta curve and scale to the right of the graph are the phase response.

Showing Group Delay

The phase response can be exchanged for group delay response by pressing the "**D**" key on the keyboard, and returned to phase with the "**P**" key. You should try this now to verify the response.

There are several other items to notice on the graphics screen. The name of the circuit that was graphed is located at the top center of the graph. To the left and right of the circuit name are the legends "REF=". The value to the left refers to the magnitude response and is shown in white. The magnitude REF gives the absolute magnitude reference of the 0dB point on the magnitude scale. For this particular graph the reference is shown as -6.0209494dB, indicating that the 0dB scale mark actually represents -6.0209494dB. There is a similar reference for the phase scale, or delay scale, whichever is presently shown. All measurements from the graph are thus normalized to the peak of the respective response curve.

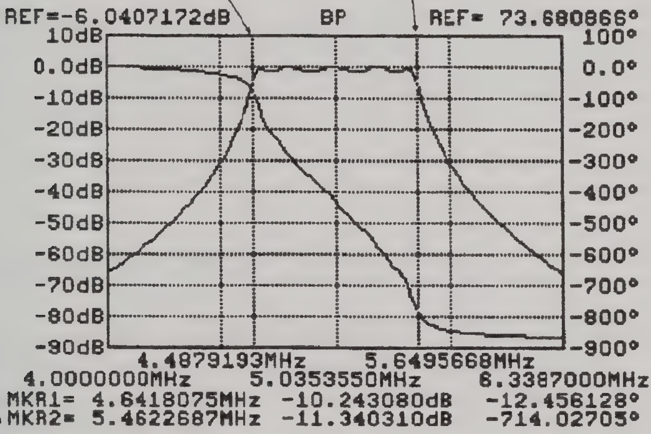
The frequency scale is given in a light blue-green (cyan) along the bottom of the graph. Five frequency increment points and corresponding graticule lines are always shown. The first and last points are taken from the circuit criteria section as the first and last points respectively analyzed. The three intermediate points are determined based upon whether the analysis was performed in logarithmic or linear increments.

Now the [F1], [F2] and [F3] function keys can be used to switch between the component, analysis and graphic screens respectively.

Graph Markers

Press the [F3] function key to return to the graphic screen if you have changed. Next, hold down the right arrow key (→). A vertical line marker is produced on the graph which can be positioned with the right and left arrow keys. The frequency, amplitude and phase of the marker position are shown in the display at the bottom of the graph next to the legend "**MKR1**".

Marker 1 **Marker 2**



```
MKR1= 4.6418075MHz -10.243080dB  -12.456128°
MKR2= 5.4622687MHz -11.340310dB  -714.02705°
```

Marker information

Figure 1-9
BP Graph with Marker Information Added

Pressing the "2" key at the keyboard upper row will select the second line marker as active. Now the arrow keys will move marker 2 to pinpoint a second frequency, amplitude and phase point on the graph as shown in Figure 1-9. Note that when marker 2 is made active, marker 1 remains on the screen.

Pressing the "1" key returns control to the 1st marker.

The up arrow key (↑) seeks the maximum response point on the graph for the specific marker active and the down arrow key (↓) seeks the minimum. For maxima and minima search purposes the two markers have slightly different attributes. Marker 1 is associated with the magnitude response and is shown in the same color as the magnitude response curve. Marker 2 is associated with the Phase or Delay response, whichever is presently displayed and again is shown in that color. These markers are very handy for highlighting specific points on the graph.

To remove one of the markers, use the **[Home]** or **[End]** key to move it to the left or right edge of the graphic screen. When off the screen, the marker information at the bottom of the graph is also removed.

Changing the Circuit

Suppose now that you wanted to change the circuit to determine the effect of component variance or to try a slightly different design. LCAS has several methods available for modifying the circuit and components:

1. Component values
2. Component nodal connections
3. Copy, insert and delete components
4. Automatic node renumbering

In this example we will only try the first two of these types of changes. The second sample session will include further examples covering the copy, insert, delete and renumbering commands.

One purpose of showing the following circuit modification techniques is to demonstrate what can be done with the new information when graphing.

The following description assumes that you have just finished analyzing and graphing the "BP" circuit as described above. If you have not, or have been experimenting with other functions, repeat the example instructions to arrive at a fresh analysis and graph of the BP circuit. Then return to the Component screen using the [F1] function key.

First try changing the value of component #3, the inductor between nodes 2 and 0, by placing the cursor over the existing value (1.0000 uH) and typing in a new value, say 3.0 uH. The "micro" multiplier is the "U" key. The full sequence is then -

3u [Return]

and the new value is entered.

Notice that none of the other entries for this component changed by changing the component value. This is true for any component entry change except the component "type", which, when changed requires re-entry of all items. Changing the "Type" designation also deletes the component that previously held that position, and replaces it with the new component being entered.

Now you might want to see the effect of this change on the circuit's response. First analyze the circuit again using the [F5] function key. But this time do not graph the response using the [F6] function key, as this will replace the previous graph. Instead the new response can be overlayed on the previous graph. To overlay the graph give the slash command -

/GOP

for Graph, Overlay, Present. Both response curves are now displayed as shown in Figure 1-10. There is no limit to the number of graph iterations that can be overlayed in this manner.

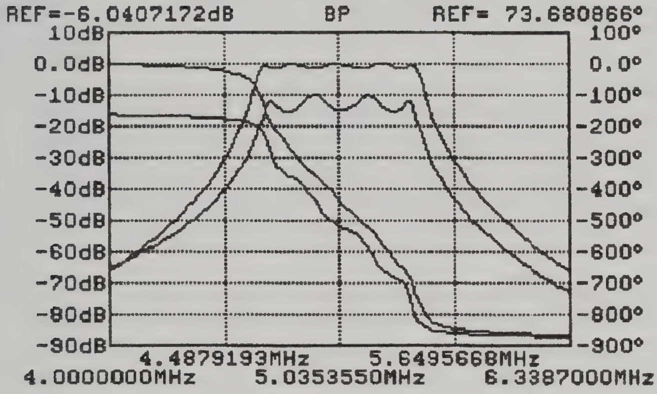


Figure 1-10 Overlayed Graph

Before proceeding to the next step, return the display to its initial state by changing the value of component #3 back to 1.0 uH and analyzing and graphing again with the **[F5]** and **[F6]** function keys.

There is another method to change component values in LCAS which is very convenient when trying to determine the effect of tolerances. A percentage change can be added to or subtracted from a component value by placing the cursor on the value and typing the percent change desired followed by the "%" key and **[Return]**. A positive or negative value can be used. For instance to reduce the value of component #4, the capacitor between nodes 2 and 3, by 10%, you place the cursor over the present value and type -

–10% [Return]

The value will change from 10.0 pF to 9.0 pF. Next analyze the circuit again using the **[F5]** function key. This time you may

want to see the difference in response of the circuit directly displayed. The command to present this graph is -

/GNS

representing Graph, New, Subtract(Last-Present). This will present a new graph instead of an overlay as in the previous example, and subtract the present analysis results from the last to generate the new graph. After having a look over the graph return to the component screen using the [F1] function key.

To return to the former value of a component after a percentage change might normally require a little thought, but LCAS provides a simple method of reversing a percentage change. To do this simply repeat the last command but precede the percent change by the letter "R". Thus to reverse the -10% change above, type -

R-10% [Return]

and the component will return to its original value, 10.0 pF.

Now return the analysis results and graph to their original states by issuing the commands to re-analyze and graph -

[F5] and [F6]

Expanded Analysis

The graph of the BP circuit response we have seen so far shows the response over a wide enough frequency range to detail overall performance. It is sometimes useful to view certain portions of a response in a close-up or expanded mode. This is like zooming in on a section of a graph for a more detailed view.

Obviously you could go to the circuit criteria section and change the start and stop frequency points to re-analyze over a smaller frequency range. Instead, LCAS provides a much simpler

method of performing an expanded analysis with the advantage that the original start and stop frequency limits are maintained. The new limits of analysis are chosen directly from an existing graph.

To prepare for an expanded analysis, we use the graphic markers when viewing the graphic screen to "bound" the frequency range of interest. There are three possible variations that can be employed here:

1. If only Marker 1 is visible on the screen, the frequency range is taken from the normal start frequency up to the Marker 1 set point frequency as displayed at the bottom of the graph.
2. If only Marker 2 is visible on the screen, the frequency range is taken from the Marker 2 set point frequency as displayed at the bottom of the graph up to the normal stop frequency.
3. If both markers are visible on the screen, the frequency range is from the lower marker to the upper marker. It does not matter what order the markers are set.

Set both markers on the graph to bound the frequency range of the magnitude response in the filter passband right up to the edges of the response. The marker frequency set points should be approximately at 4.6418MHz and 5.4622MHz.

Now use the following slash command -

```
/AE [Return]
```

representing Analyze, Expanded. You cannot use the [F5] key to accomplish an expanded analysis.

When the analysis is completed press the [F6] key to graph the new expanded response data. After pressing the "D" key to show delay, the new graph should look like the one in Figure 1-11. Note that the label "EXPANDED" is shown across the top of the graph.

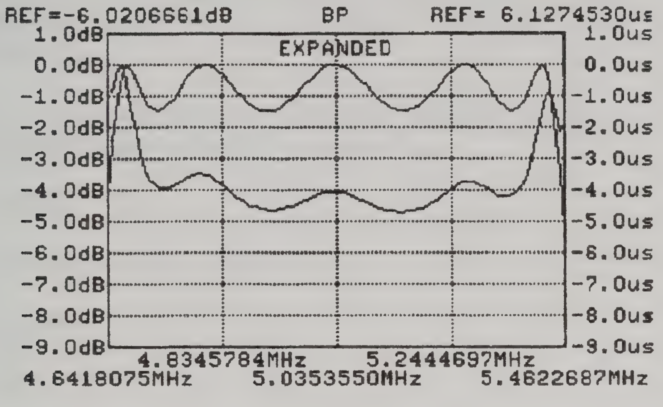


Figure 1-11
Expanded Analysis with Group Delay

The delay response shown is the group delay across the passband of the filter.

Manual Scale Mode

In all the examples so far the vertical scales for magnitude, phase and delay have all been automatically chosen by LCAS to display all of the data available. These scales can be overridden and the scales set manually by selecting the "Set Scale Mode" from the /Graph menu. You are then prompted for either Automatic or Manual scales. When you choose one of these options it is set until changed again by re-selecting the "Set Scale Mode".

After setting the scale mode you are returned to the main Graph menu where you continue to choose the type of graph desired. Whenever in the manual scale mode, you are prompted to set

the scales desired immediately before graphing unless you chose the overlay option. Overlays require that each graph use the same scales

To manually set the magnitude scale on the BP graph, first set the manual scale mode with the command -

/GSM

for Graph, Set Scale Mode, Manual.

then enter -

NP

for New, Present only. At the new prompt choose -

M

for Magnitude. When prompted for the maximum magnitude level to display just hit **[Return]** to select the default of -6.02dB. At the prompt for minimum level, type in -

-7.5 [Return]

Now select -

V

for View Graph and the graph will be displayed with your new magnitude scales as shown in Figure 1-12. This graph is a combination expanded analysis with manual magnitude scales showing detail of the ripple in the BP circuit passband.

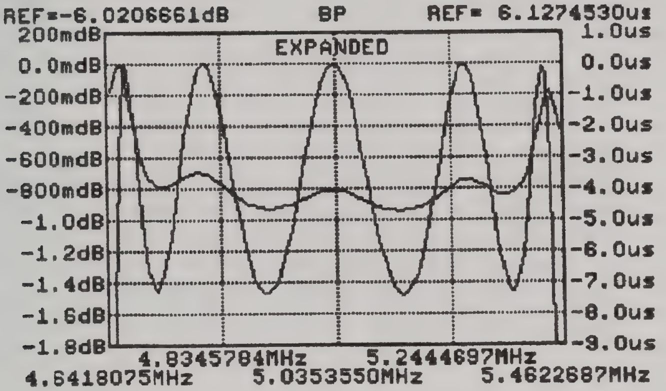


Figure 1-12
Expanded Analysis of the BP circuit with Manual Scales

Noise Power Display

There is one more important feature of LCAS we can show using the "BP" circuit, the noise power display. It is common practice for filters used in communications and measurement circuits to be described by their effective "noise bandwidth" or the amount of total noise power they represent. For instance, a spectrum analyzer display of signal-to-noise ratio requires a knowledge of the effective noise bandwidth of the filter used to limit the noise. Knowing that, the true signal-to-noise ratio in any bandwidth can be calculated.

In LCAS the noise power and a derived noise bandwidth is calculated as the integral of the power represented by the magnitude response, or the "area" under the curve of the magnitude response. To better show this first re-analyze and graph the "BP" circuit using the -

[F5]

and

[F6]

keys. Then place marker 1 at the peak of the magnitude response. The easy way to do this in LCAS is by pressing the up arrow key with the graph as the current active screen. By the way the down arrow seeks the minima of the response, and marker 1 works on the magnitude response while marker 2 works on whichever of the phase or delay response presently displayed.

Now press the "N" key, representing "Noise" and a new line will be displayed at the bottom of the graphic screen as -

```
Pin=1.0W/Hz   Pout=174.18kW   -MKR1=699.96kW
```

The first entry, Pin, indicates that the normalized input power to the circuit was noise at a power density of 1.0Watt per Hertz. The Pout of 174.18 kiloWatts indicates the total noise power at the output of the circuit. The Pout figure includes the circuit loss of approximately 6 dB from input to output. The third number (-MKR1) is the power out minus the level of the response at marker 1. Since marker 1 was set at the peak of the magnitude response within the passband then this number represents the power output normalized to the passband. This would have significance since a signal within the passband of the filter would suffer the same 6dB of loss.

The figure computed for Pout - Marker1 also represents the noise bandwidth of the circuit where 1 Watt represents 1 Hertz of bandwidth. Consider for example that this circuit's magnitude response was a perfect function with a flat passband response and vertical lines representing "brick wall" band edges. The number of watts at the output relative to marker 1, again in the passband, would actually be equal to the number of Hertz of bandwidth since there is 1 Watt per Hertz. The same is true of

the "BP" circuit response. The noise bandwidth of this circuit is 699.96 kHz.

Whenever the graphic screen marker 1 is moved the noise power display will be removed. To display the noise power again or to re-compute the noise power at a new marker 1 level, just press the "N" key again.

Area Under Curve

A variant of the noise power display can be used to find the power in a certain portion of the graph response. For example a filter response might have a slight "bump" in level in the stopband and you wished to know how much power this represented with respect to the passband.

The two graphic markers are used to bound the frequencies of interest. Then by pressing the "A" key the absolute power represented by the magnitude response between the two markers is computed and presented on the bottom line of the graph screen.

By bounding first one area of the graph and computing power, and then a second area, the relative magnitudes or ratio of powers can be easily determined.

Calculation of Effective Jitter

A common calculation in the design of circuits for communications and test equipment is the effective jitter represented by thermal noise impressed on a carrier or desired signal. This type measurement is usually done on phase locked loop circuits which generate the system carriers. For those who perform such calculations, LCAS has a built in function which will calculate

the jitter in degrees and radians represented by the energy in a defined frequency range.

Before using the Jitter function the power in the area of interest must be calculated using either the Noise power function or the Area function. Then the jitter function calculates the jitter represented by the displayed noise power by pressing the "J" key. Only the noise power figure of the Noise function are used, not the "-MRKR 1" figure. All the features of the Area (integration) function are used in the noise and jitter calculation such as using the two graphic markers to bound the frequency range of interest.

The jitter calculation has no relation to the circuit we are presently analyzing, but an example of using the jitter function in a phase locked loop application is given in Appendix D.

Nodal Circuit Representation

Now that you have a basic idea of how LCAS itself is manipulated you should back up and consider the method used to represent electronic circuits within the LCAS environment.

The following description assumes the reader is familiar with the basics of electronic circuits and design and with schematic representation of circuits. If not there are many good texts on electronic circuit design available. LCAS will not design circuits for you. LCAS is a designer's tool used to simulate and analyze an already existing or new circuit design.

The term "Node" is used to denote the circuit connection point for component leads.

LCAS performs a nodal circuit analysis. It is therefore necessary to enter circuit information into LCAS in a nodal representation. This normally means little more than numbering the nodes on a schematic diagram. Unless a circuit contains only two or three components, a schematic diagram of the circuit to be analyzed is invaluable when using LCAS. Without the schematic it is too easy to miss a component or connection and derive incorrect answers. Like most computer tools, LCAS can only provide valid results with correctly entered information.

Direct keyboard numeric input is used to describe a circuit in LCAS. This method offers several real advantages over a schematic drawing method. Foremost it is much faster than any of the "schematic capture" type programs used in CAD systems. Second, circuit files are compact and typically man-readable. Third, compatible circuit files can be generated by external programs, using common techniques such as filter synthesis, and interchanged with LCAS.

Numbering the Nodes

An example circuit diagram is shown in Figure 1-13. The nodes are numbered consecutively from circuit input to output. The actual analysis computation is not dependent on the node numbering order, but many editing functions depend on this consistency for ease of use. If the nodes of each functional area of a circuit are consecutively numbered, then this group of nodes can be easily manipulated as a single object, saved as a separate circuit, and later brought into other circuits as a merged module. More sophisticated commands, such as copy and merge, do require the circuit nodes to be numbered consecutively from input to output for best results.

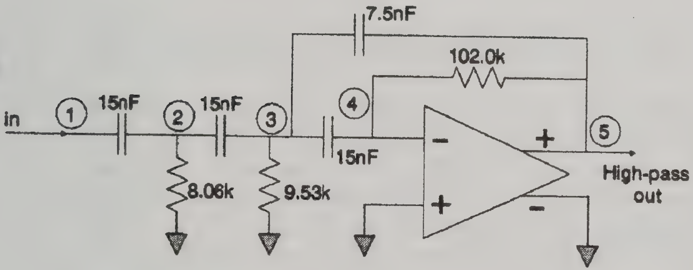


Figure 1-13
Sample Circuit with Nodes Numbered

The sample circuit shown is an active high-pass filter containing several different component types. We will see more of this filter type in the next example work session.

Node numbering normally begins with the digit 1. Node 0 is assumed to be the ground or common node, and is also used for all power supply connections.

All nodes used, except the input and output nodes, must have more than one component lead connected or an error is reported. Node numbers cannot be skipped without also causing an error to be reported.

A specific component in LCAS is identified by its type, value and nodal connections. Components are not numbered by type as in a typical schematic, such as C1, C2, R34.

Changing Nodal Connections

Changing the circuit nodal connections is accomplished by placing the cursor over the desired node and typing in the new nodal connection.

Input and Output, Source and Termination

All circuits used with LCAS have an input and an output node. The input node is the excitation point for the circuit, and the output is where analysis information is recovered. LCAS provides a common input excitation. It is a 1 Volt RMS voltage source, with 0 Ohm output impedance. The determination of the source impedance and the necessary components to represent it is your responsibility.

The circuit of figure 1-13 required no source or terminating impedance as it is intended to be driven from a low impedance source and to provide a low impedance output. Many circuits do however require that they be connected to proper impedances at both input and output. For instance, an IF filter for communications use would probably require a 75Ω source impedance, and the first component would then be a series 75Ω resistor from node 1 to node 2. An alternative source impedance circuit is shown in the appendix "Tips and Techniques".

The output node is the circuit point at which LCAS provides analysis information. The output information is relative to the

input node. The designation of a node as the output presents no load to the circuit. If a circuit requires a termination at the output, it must be specifically placed there. For instance, typical RF circuits commonly require a 50Ω termination impedance. Therefore a 50Ω resistor is placed between the output node and ground. Figure 1-14 shows a circuit with properly terminated inputs and outputs. For another example refer back to the BP circuit shown in Figure 1-6.

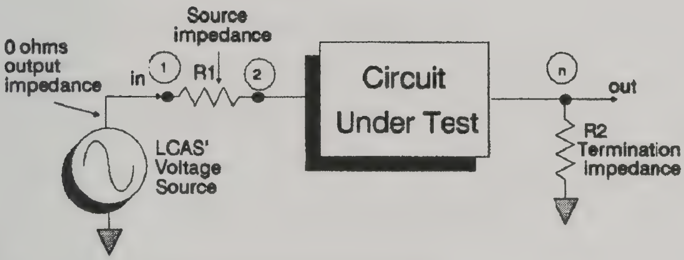


Figure 1-14
Circuit Source and Termination Impedance

The input and output node designations in LCAS can be changed at will to analyze a circuit from different points. For instance, if the output response of a circuit was not as expected, then perhaps one or more intermediate nodes can be checked to determine where the response varies from expectation.

A circuit with multiple outputs can be analyzed sequentially at each of the output nodes and compared. For instance a hi-fi crossover network might have 2 or 3 outputs, each designed to cover one frequency range. The outputs can be displayed as graph overlays to determine relative responses and phase matching. Just such a circuit will be analyzed in the next example session.

Example Session Two -

Entering and Manipulating Components.

This next example work session will show more details of using the component editor to:

- Enter a circuit description.
- Saving circuit files.
- Deleting components.
- Copying components.
- Renumbering component nodes.

In addition the example also includes:

- Circuit analysis with multiple outputs.
- More on overlaying graphs.

The circuit chosen for this example is a hi-fi crossover network which could be designed into an amplifier. The circuit has dual outputs designed to drive two output amplifiers which are connected to separate loudspeakers.

The schematic diagram of the crossover network is shown in figure 1-15. Notice that the circled node numbers begin at 1, which is the input node. There are two outputs available, at nodes 5 and 9

Figure 1-15 represents the first step in any analysis with LCAS, which is to have a circuit diagram in front of you with the nodes numbered.

The second step is to enter the circuit description into LCAS using the component editor. Most of the components have al-

ready been entered into the Crossover Network circuit file located on disk under the name "XOVR-EX", so first load that file using the commands you learned in the first example.

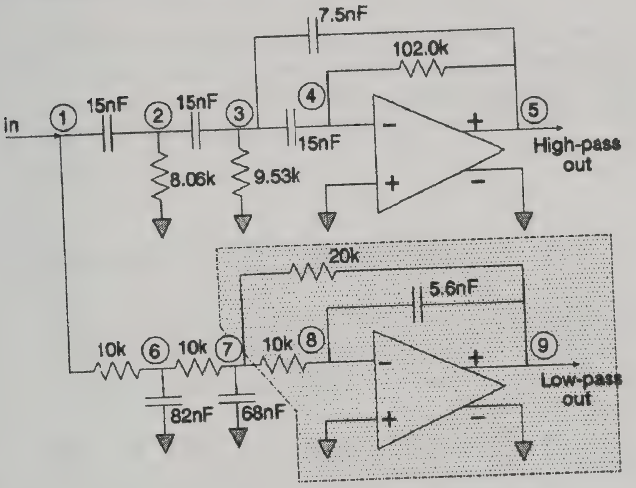

7.5nF
102.0k
in
①
15nF
②
15nF
③
④
15nF
8.06k
9.53k
⑤
High-pass out
20k
5.6nF
10k
⑥
10k
⑦
10k
⑧
⑨
Low-pass out
82nF
68nF

Figure 1-15
Crossover Network Schematic Diagram

You will only be adding those components shown in the shaded box on the schematic, including two resistors, a capacitor and an operational amplifier.

Just in case you've forgotten you can load the circuit with the command -

[F9] {Continue to display file} L

then move the cursor over the file named "XOVR-EX" and press -

[Return]

Next place the cursor on the first empty row of the "Type" column at the bottom of the existing component entries. The **[End]** key will take the cursor directly there.

Have another look at the circuit and note that it is composed of two paths which separate at the input node. Considering that this is a crossover network the two paths represent the high-pass section in the upper path and the low-pass section in the lower path.

Entering the First Component

The first component you will be entering is the resistor in the low-pass section between nodes 7 and 8. Components are entered by typing the highlighted letter of the component name as shown in the menu/prompt area of the screen. If any of the "slash" command prompts are presently displayed instead of component names, just press **[F10]** to return to the main command level. If the component you are interested in is not shown, press "**M**" to show another line of the menu. Since we want to enter a resistor type an -

R

for resistor. The "Type" column will now display "**Res**" and the cursor will proceed to the first cell of the "Specification" column. The command cell now prompts you to input the "Value in Ohms?". A quick look back at the schematic shows that the resistor's value is 10k Ohms, so enter -

10k [Return]

Notice that as you type the Command cell shows what you have entered so far. You can use the backspace key to change a typing error anytime before striking **[Return]**. When you are finished with the entry LCAS places "Val = 10.000kΩ" in the cell and proceeds to the next.

Next we enter the "From Node" as -

7 [Return]

and the "To Node" as -

8 [Return]

That completes the entry of the first component, and it was easy.

Try entering the capacitor now between nodes 8 and 9. Notice that after entering the value of the capacitor, the command cell asks for "Value" and the menu/prompt line says "Quality Factor 1.0000a < Value < 1000.0T 0=Infinite Q". LCAS wants to know what the Q of the capacitor is. There is a full discussion on "Q" in Part 2 and for now let us assume that the capacitor is ideal, so just press -

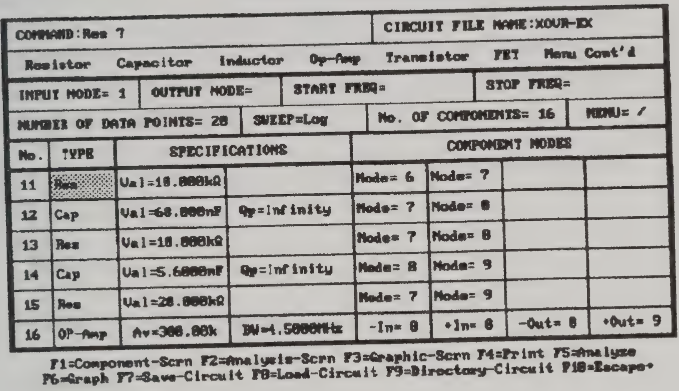
[Return]

You should be able to enter the remainder of the components in the circuit yourself knowing that the amplifier has an open loop gain of 300,000 (Av = 300k) and a unity gain bandwidth of 4.5MHz. Then just keep the following points in mind:

- You can back up during a cell entry using the backspace key.
- You can back up during a component definition before all cells are completed by using the left arrow or **[Esc]** key.
- After a completed component definition, you can change any value by placing the cursor on the desired cell and entering the new value.
- The ground or common is node 0.
- All component nodes must be connected.
- The unused negative Op-amp output is connected to node 0.

When you are finished the end of the component list should look like that in figure 1-16, showing components 13 through 16

which you just entered. If it doesn't then you should make the necessary corrections before proceeding to the next part of the example.



COMMAND:Res 7	CIRCUIT FILE NAME:XOVR-EX

Resistor Capacitor Inductor Op-Amp Transistor FET Menu Cont'd

INPUT NODE= 1	OUTPUT NODE=	START FREQ=	STOP FREQ=
NUMBER OF DATA POINTS= 20	SWEEP=Log	No. OF COMPONENTS= 16	MENU= /

No.	TYPE	SPECIFICATIONS		COMPONENT NODES			
11	Res	Val=10.000kΩ		Node= 6	Node= 7		
12	Cap	Val=68.000nF	Qp=Infinity	Node= 7	Node= 0		
13	Res	Val=10.000kΩ		Node= 7	Node= 8		
14	Cap	Val=5.6000nF	Qp=Infinity	Node= 8	Node= 9		
15	Res	Val=20.000kΩ		Node= 7	Node= 9		
16	OP-Amp	Av=300.00k	BW=4.5000MHz	-In= 8	+In= 0	-Out= 0	+Out= 9

F1=Component-Scrn F2=Analysis-Scrn F3=Graphic-Scrn F4=Print F5=Analyze
F6=Graph F7=Save-Circuit F8=Load-Circuit F9=Directory-Circuit F10=Escape+

Figure 1-16
Crossover Network Component List

Just to be safe you should now save the crossover network circuit description to disk. Then if something really drastic happens it can be easily recovered. To save the file use the slash command -

/FS

You will be prompted to save the file under the existing name that the circuit file was loaded with, XOVR-EX. Since we want to use a new file name enter -

MYTEST [Return]

to save the circuit under the name "Mytest". LCAS adds its own file name extensions automatically.

Circuit Criteria Entry

There is a little more information needed before the crossover circuit can be analyzed. The Circuit Criteria section must be completed to show LCAS the specifics of how you want the circuit to be analyzed. Press the **[Home]** key twice to go to the top of the circuit criteria section.

The first entry required is the circuit input node. We know this is at node 1 so enter -

1 [Return]

Then move to the "Output Node" cell and enter -

5 [Return]

to look at the response of the high-pass section. Next enter the start and stop frequencies as 20Hz and 20kHz respectively. Select 50 data points and finally request a logarithmic increment for the analysis steps. This is usually best when the frequency range of start to stop is several decades as this is. To enter the logarithmic sweep mode you use the letter "N" as prompted for non-linear.

The circuit was already saved once after the component list was completed. You should now save the circuit again after the circuit criteria section is complete. This new information will be saved with the file and is available whenever the circuit is loaded. This time though you do not have to enter the circuit name, just press -

/FS [Return]

or

[F7] [Return]

You will be asked to confirm replacement of your original "MYTEST" circuit file by pressing -

Y

for yes.

Analyzing the Test Crossover Circuit

We are going to show several methods to analyze and manipulate the circuit you just entered. First we will:

- Analyze the high-pass section and graph.
- Analyze the Low-pass section and overlay this graph.

Next we will re-analyze the circuit, but in pieces to show different functions. We will:

- Delete the low-pass components and analyze the high-pass circuit by itself.
- Delete the high-pass components (1 through 8).
- Renumber the remaining low-pass components.
- Analyze the low-pass circuit by itself, overlaying this graph.

This exercise will show how to use the Delete and Renumber commands and analyze circuits in sections. Although this sounds like a lot of work, you will be amazed at how quickly it goes, so let's get started.

First make sure that the circuit criteria is set correctly to analyze the crossover circuit over the high-pass section from node 1 to node 5. Then analyze and produce a new graph of the data by pressing the keys -

[F5]

and then when the analysis is completed -

[F6]

which will produce a graph with a high-pass type response as shown in figure 1-17.

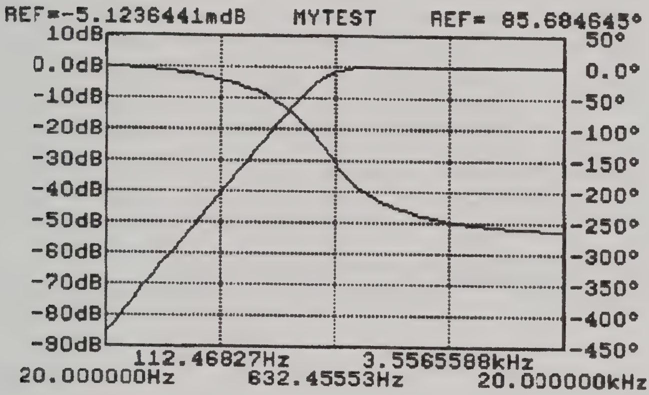


Figure 1-17
Graph of the Crossover Network High-Pass Section

Next, change the output node specified to 9 in the circuit criteria section. Then press -

[F5]

again to analyze the circuit from node 1 to node 9. Now we want to overlay the graph of this new section on the previous graph, so the command is -

```
/GOP
```

A picture of the composite graph is shown in Figure 1-18, showing that the magnitude responses of the two circuit paths complement each other to deliver equal levels across the audio range from 20Hz to 20kHz.

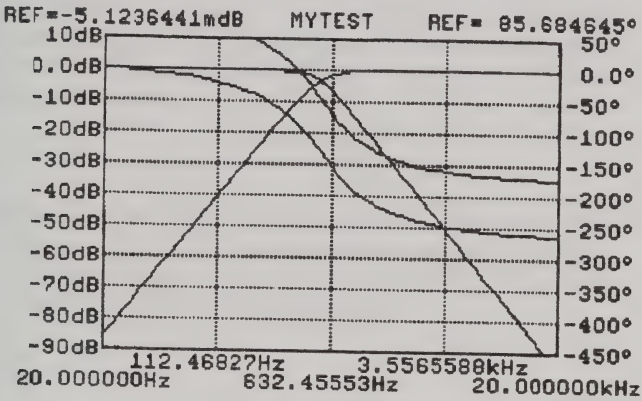


Figure 1-18
Composite Graph of the Crossover Network

Notice in the composite graph that the low-pass phase response is not shown below about 200Hz. LCAS "clips" response data of overlay graphs which do not fit within the scales of the original graph displayed. All of the information can be shown by using the manual scale mode on the first graph, or in this particular case by graphing the low-pass section of the circuit first.

Deleting Components

Now let's try again a different way. Return to the component editor using the [F1] function key. We will first delete the low-pass section from the component list and analyze only the high-pass section. Place the cursor on the first component of the low-

pass section which is the resistor between nodes 1 and 6 (component No. 9). Now start the delete process by giving the slash command -

/D

and the entire component line will be highlighted. Press the down arrow key until the highlighting includes all components from No. 9 through 16. The highlighted components are now defined, and you press -

Y

to confirm that these are the components to delete. They will now disappear and are not recoverable except from the circuit file on diskette. Go up to the circuit criteria section and set the output node to 5 and analyze the circuit using -

[F5]

Notice that the analysis is much quicker with only one half the number of nodes. Make a new graph using the -

[F6]

function key, which should be identical to the graph produced previously over the same circuit path.

Now we want to separately analyze the low-pass section of the circuit, but we deleted it. We must get it from the disk file containing the full circuit. Load that file again using -

[F9] {Display page with "MYTEST"} L
{Cursor to "MYTEST"} [Return]

This time we will delete the high-pass components numbered 1 through 8, by placing the cursor on component 1 and pressing -

/D {Cursor down to include No. 8} Y

The remaining components are those we wanted but the node numbers now skip 2 through 5. Just to see what happens press

the [F5] function key to analyze and LCAS complains with a beep and the message "NODE 2 SKIPPED".

Renumbering Component Nodes

We have to renumber the nodes remaining consecutively from 1 without skipping any numbers.

Place the cursor on the first component and give the renumber command -

```
/R {Cursor down to component No. 8} Y
```

Now we are asked for a number to add to each of the node numbers in the existing component definitions. Since we want node 6 to become node 2 and node 9 to become node 5, the number to add is -4 (minus 4). Our response to the prompt is -

```
-4 [Return]
```

This example was specifically chosen to show a point that must be watched for. The original resistor between node 1 and 6 has had 4 subtracted from its node numbers. One end of the resistor is now tied to ground! This is an unusual case because renumbering typically involves adding numbers to the middle of a circuit. But, in this case we have made an error that must be corrected by placing the cursor on the first node of the resistor and changing it to 1. Do that now with the entry -

```
1 [Return]
```

Then analyze the circuit using -

```
[F5]
```

and overlay the graph with the command -

```
/GOP
```

Our graph should be identical to the first composite produced as shown in Figure 1-18.

To show that there is always one more way to look at a circuit, you can try the following exercise on your own. Sum the high-pass and low-pass outputs of the crossover network by connecting nodes 5 and 9 each through a 1k OHM resistor to a new node 10. Using node 10 as the output will give a combined frequency response.

This completes the second example. Although we covered a lot of ground, it should have gone quickly. If you experienced problems with any of the exercises in either the first or second example sessions, you should go back and try to discover the reasons now. If a review of the example does not resolve the problem, then consult the Command Reference in Part 2 for more information.

Conclusion

Several other sample circuit files are supplied on the master diskette. Look through some of these files to see how typical circuits are built in LCAS and their response characteristics. More information on many of the sample files is included in Appendix F, Example Files.

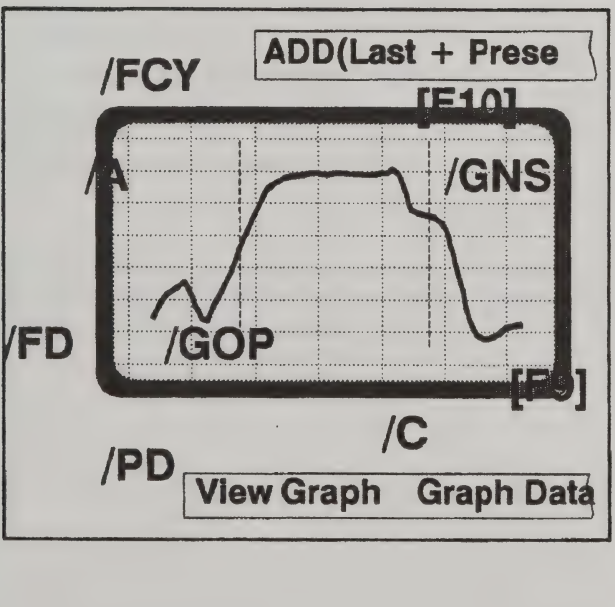
Don't be afraid to try any of the functions explained so far or to experiment with other functions and commands. There are very few ways to lose information that has already been saved in a circuit file on diskette. That's also the purpose of making a backup of the master diskette.

If you've been following Part 1 from the beginning you now know most of the basics for operating LCAS. The reference material in Part 2 should now be read once to see all the capabilities and commands available within LCAS. Later, when you need a little help you should only require a quick refresher in Part 2 and Part 3, or the command summary in Part 4.

You should also look over the Appendices covering several subjects, especially those entitled "Often Overlooked Features" and "Tips and Techniques". If you work with Phase Locked Loop circuits then Appendix D on PLL modeling techniques and examples will be most interesting.

PART 2 -

COMMAND REFERENCE


ADD(Last + Prese
/FCY
[F10]
/A
/GNS
/FD
/GOP
[F9]
/C
/PD
View Graph
Graph Data

Introduction

This section of the LCAS manual is less tutorial than Part 1, but is still descriptive of command sequences required to accomplish common functions or activities. This is to provide for easier referencing of information after you are familiar with the basics of LCAS.

This command reference begins with a discussion on issuing commands and the menu structure. After that the order of covering subjects is the same as the general order of performing an analysis. That is:

1. Component entry
2. Modification of components and circuits.
3. Managing Circuit files.
4. Analysis, including setting the analysis criteria.
5. Variations of Graphing data.
6. Outputting data to printers and files.

Figure 2-1 depicts the typical steps in the process of analyzing a circuit with LCAS, and shows the relationship between the major sections of Part 2 of this manual.

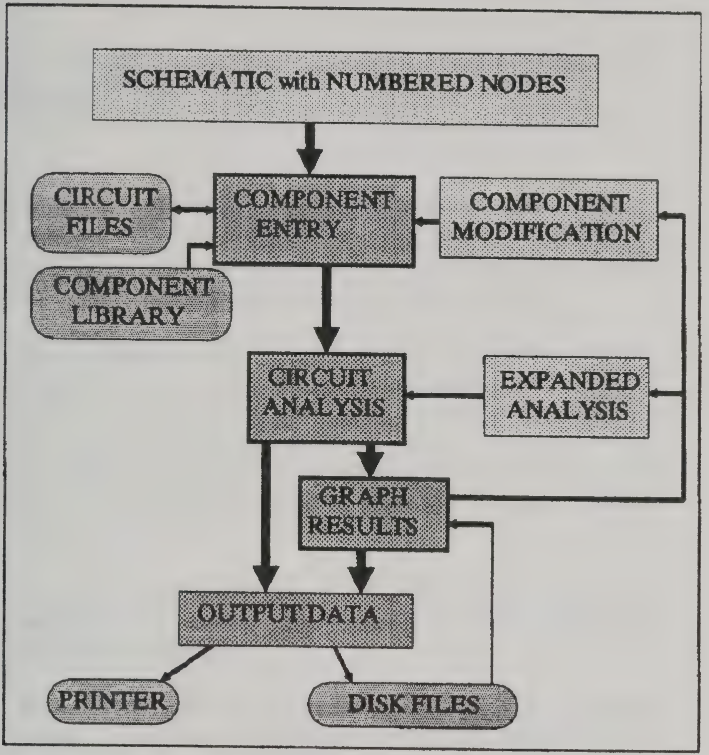

SCHEMATIC with NUMBERED NODES
CIRCUIT FILES
COMPONENT ENTRY
COMPONENT MODIFICATION
COMPONENT LIBRARY
CIRCUIT ANALYSIS
EXPANDED ANALYSIS
GRAPH RESULTS
OUTPUT DATA
PRINTER
DISK FILES

Figure 2-1 Circuit Analysis Process

Each major topic is covered as a stand alone description so that the user may refer to this material later and get a complete picture of commands and their related context.

Command Structure

LCAS is a command driven program which presents a menu of available commands in the menu/prompt line of either the component or analysis screens. A discussion of these terms is contained in Part 1 under the section title "First Encounter".

The underlying command mode when in the component screen is assumed to be component entry or modification. This mode is depicted by the component list in the menu/prompt line when not in the process of executing a command and the cursor is in the component definition section of the screen. When the cursor is in the circuit criteria section LCAS is set to enter or modify data in those cells.

When the analysis screen is active LCAS is set to review the analysis data, or enter or modify data in the circuit criteria section of the screen only.

When the graphic screen is active LCAS is set to execute graphic commands. These include setting the graphic markers and the display of phase, delay, noise power and area under the curve.

Command inputs can be of three types when there is not an existing command in process. Commands are chosen by pressing:

1. A highlighted letter selecting one of the options in the menu/prompt line or,

2. A function key selecting one of the options on the lower function key reminder lines or,

3. Striking the slash character, "/" which brings up a new command menu in the menu/prompt line.

The slash command menu is:

```
Analyze Graph Copy Renumber Delete Print Files Set-up Quit
```

Notice again that in our text and also on your screen the first letters of the words on the Menu/Prompt line are displayed in bold indicating the key to press for that option.

Backing Up Within Commands

Pressing the **[Esc]** ("Escape") key causes the command level to pop back one level, effectively "backing up". The **[F10]** function key is a quick way to abort any pending command and return to the main command level.

Quitting LCAS

Quitting LCAS returns to the DOS operating system. To quit LCAS use the slash command -

```
/QY
```

representing the quit command followed by a "Y" response to the prompt "Exit (Y/N)?". Any information not saved to disk is lost when LCAS is quit.

The LCAS program version number and serial number are displayed at the same time as the confirmation prompt when the quit command is invoked.

Set-Up Command

The Set-Up command is covered in Part 1 under the section titled "First Encounter", "Configuring LCAS".

COMPONENT ENTRY

Component entry is the process of defining a circuit for use in LCAS. Component entry assumes that you have previously generated a circuit schematic with the nodes numbered according to LCAS conventions. See Part 1 for more information on numbering nodes.

All component entry is accomplished in the "Component Screen". This screen is the first displayed when entering LCAS and after loading a circuit file. If presently viewing either the analysis screen or the graphic screen, the component screen may be selected as "active" by pressing the **[F1]** function key.

If a circuit file is presently in the component screen and it is desired to start a new circuit file, the existing components can cleared from memory using the "Clear" slash command -

```
/FCY
```

LCAS will automatically clear the screen and memory of any existing components on initial start-up and before loading a new circuit file from disk.

Component entry can be accomplished with or without a circuit file in memory. If a circuit file is already in memory new components are added to those existing. The circuit file on diskette from which a circuit in memory was loaded is not modified however until the circuit is saved to disk under that file name.

Entering components affects only one cell of the circuit criteria section of the screen. That is the "No. OF COMPONENTS" display is automatically updated to show the current number of components in the circuit description.

The component menu and prompt should be visible in the menu/prompt line (second line on the screen). If during component entry other commands have been used it may be necessary to press **[F10]** to return to the main command level showing component types in the prompt. The component menu/prompt will only be visible if the cursor is placed on a "Type" cell.

Pressing the "**M**" key will show a second line of component types available and is used to toggle between the two prompt lines. The two component menu/prompt lines are:

Resistor Capacitor Inductor Op-Amp Transistor FET Menu Cnt'd

and

X-former T-line OT-line ST-line ϕDet Loop-Amp VCO ÷ N Menu

Most of the component can be selected even when it is not in the presently visible component menu. The exception is those components beginning with "T" or "O" since there is more than one component selection which uses those letters.

Starting a new Component Entry

To enter a new component, or add a new component to an existing circuit, the large inverse cursor is placed on the first available blank component "Type" cell at the bottom of the component listing. The cursor will go to this blank cell by pressing the [End] key (twice if the cursor started in the circuit criteria section). Then one of the letter keys is pressed representing the desired component as shown by the highlighted letters in the menu prompt. If the desired component is not in the present menu, press "M" to switch to the other component menu.

For instance to enter a resistor press the "**R**" key. Watch the cursor and the prompt line change to prompt for the next required entry, which in this case is the value of the resistor.

If you accidentally pressed the wrong key then back up by pressing the **[Esc]** key to "escape". The left arrow key can also be used to escape from the last entry. Any time before the completion of all entries for a component the **[Esc]** or left arrow can be used repeatedly to erase entries, i.e. to erase the last two entries press the **[Esc]** twice.

Value Entries

LCAS accepts component values in common *engineering* terms, or in *scientific* notation. Suppose a resistor is to have a value of 4700 ohms, or in standard engineering units 4.7k ohms. Simply enter "**4.7k**" and press the **[Return]** key to enter this value. LCAS already knows it is ohms since a resistor is being entered. You could have just as easily entered 4700 or .0047M or 4.7e3. The letter "**e**" is the scientific notation indicator and means the following number is the exponent of 10.

> *NOTE: The right arrow key may be substituted for the* **[Return]** *key in any cell entry. Both result in accepting the entry and moving to the next cell entry to the right.*

LCAS accepts a full range of common multiplier designators. The only point where LCAS differentiates between upper and lower case is:

A small "m" means milli- and a large "**M**" means Mega-

For all designators except the letter "M", LCAS will accept either upper or lower-case entries.

The accepted list of multipliers is given below.

Letter	Name	Power of 10
a	ato	-18
f	femto	-15
p	pico	-12
n	nano	-9
u	micro	-6
m	milli	-3
none	---	0
k	kilo	3
M	Mega	6
G	Giga	9
T	Tera	12

LCAS formats each numeric input and fits it to the nearest power of 10 in factors of 3 as shown above, resulting in a mantissa between 1 and 999, using standard engineering notation. If a value is entered as ".0047M", LCAS would write the value as "4.7k".

Many values may be entered as negative numbers even though a "real" component could not normally have a negative parameter value. For instance a capacitor may have a negative value in LCAS. Frequency, time and length entries cannot be negative.

Nodal Connections

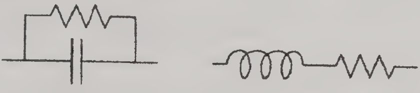
After the values and other specifications of a component are entered LCAS will ask for the node connections. Remember that node 0 is always the ground or common connection. When all node connections have been specified, LCAS is now ready to begin another component, so it returns to the "Type" column of the next line down and awaits a command.

For a discussion of the nodal description of a circuit, refer to the section in Part 1 titled "Nodal Circuit Representation".

Component Figure of Merit or "Q"

Capacitors and inductors require a "Q" to be entered. A Q entry of 0, or no entry, results in an infinite Q (representing an ideal component). A Q value other than 0 results in the addition of a resistor to the capacitor or inductor. The resistor is placed either in series or parallel with the capacitor or inductor.

The classic low frequency Q model dictates a resistor in parallel with capacitors and in series with inductors. A high frequency Q model however, might be the opposite configuration or a combination parallel and series resistor.



Classic Low Frequency Q Models

If the Q value is entered directly then the low frequency model is chosen. If the Q value entered is preceded by a "P" or "S" then the method of connecting the Q determining resistor can be forced to a parallel (P) or series (S) configuration. Once the configuration is chosen then further changes to the component Q assume the same parallel or series connection.

LCAS shows the present connection of the Q determining resistor by a "**Qp=**" or "**Qs=**" in the second specification cell for the component.

The Q determining resistor is not shown in the component list. Its value is computed at analysis time according to the part value and the frequency range of analysis. If the analysis is at linear increments then the frequency chosen for computation of Q is the analysis range midpoint or –

$$f_m = \frac{(f_{start} + f_{stop})}{2}$$

If the analysis is at logarithmic intervals then the frequency chosen for computation of Q is the geometric mean of the frequency range or –

$$f_m = \sqrt{f\ start \bullet f\ stop}$$

For capacitors the resistor is calculated by LCAS using the formulas –

$$R = \frac{Q}{2 \pi f_m C} \qquad \text{Parallel resistor}$$

$$R = \frac{1}{2 \pi f_m C Q} \qquad \text{Series resistor}$$

where f_m is the frequency calculated above.

For inductors the formulas are –

$$R = 2 \pi f_m L Q \qquad \text{Parallel resistor}$$

$$R = \frac{2 \pi f_m L}{Q} \qquad \text{Series resistor}$$

where f_m is the frequency calculated above.

LCAS uses the start and stop frequencies defined in the circuit criteria section to compute the Q resistor added to the circuit, so when an "expanded" analysis is performed, the added resistor value remains unchanged. Expanded analysis is explained further in the analysis section.

The resistors added to the inductor and capacitor described above are used to simulate the performance of real components. To properly simulate a component, especially at higher frequencies, additional parts may have to be added to the circuit in special cases. For instance at very high frequencies, inductors exhibit capacitance and capacitors and resistors exhibit inductance. When the specifications for a component do not give characteristics at high frequencies, an LCR meter or Q meter measurement of an actual component will usually give the necessary information.

Special T-Line, OT-Line and ST-Line Component Entry

The Transmission Line has four "special" versions, in addition to a standard transmission line, for simulation of real devices. The four elements are:

- Microstrip transmission line
- Coaxial transmission line
- Balanced transmission line and
- Delay line.

The Open Stub and Shorted Stub have all of these special versions except the Delay Line.

Any of these four elements are defined by first selecting the T-Line device from the standard component menu. Unless the T-Line device is displayed on the menu/prompt line then the "M" key must be pressed first to display it. The first T-Line entry prompt for the line impedance also lists "Special". By pressing "S" the new component prompt line is displayed as shown below:

```
Microstrip   Balanced Stripline   Coaxial Line   Delay Line
```

Any of these four special T-Line forms is selected in the normal fashion by pressing the highlighted letter of the name as displayed.

Modeled Components

LCAS contains standard components as part of its basic elements. The variations of actual components made however are much greater than could be contained within LCAS. Thus for very accurate representations of components, especially at fre-

quencies greater than approximately 10 MHz, a component model suitable for the particular application must be considered. If it is determined that a model is required then it is made from the elements provided within LCAS.

There are two general types of modeled components. Those which model basic elements, such as tapped inductors, and those that model specific devices, for example an LM318 op-amp. Both types are built the same way, and are discussed as appropriate in each element type in Part 3 (Component Reference).

Two basic component types covered are mutually coupled and tapped inductors discussed in the transformer element (X-former), and the Operational Transconductance Amplifier (OTA) discussed in the Op-amp element.

Phase Locked Loop Components

A unique group of components defined in LCAS are the elements of Phase Locked Loop (PLL) circuits. They provide a powerful added capability. These components may not be considered "linear" by themselves, but the complete phase locked loop they represent normally exhibits a linear response vs. frequency. The modeling of these components in LCAS gives analysis capability outside the reach of most other linear analysis tools.

The elements provided for phase locked loops are applicable to the general area of feed-back control systems of which phase locked loops are a subset.

The PLL devices included in LCAS are:

Phase Detector
Loop Amplifier
Voltage Controlled Oscillator
Divide by N

The uses and design of phase locked loops is beyond the scope of this manual. For more information on the design of phase locked loops, consult textbooks available at your local technical library, or from component manufacturers. Appendix D of this manual contains a mini-tutorial on the use of PLL components within LCAS. That Appendix also contains many examples of modeling typical phase locked loop components.

CIRCUIT MODIFICATION

Circuit and Component modification is a normal part of the engineering and testing of a circuit. It helps you discover the effect of component value changes with temperature or aging. It can also give a graphic representation of the affect on circuit performance due to component changes. The ease with which components and circuits can be modified adds a "what if" capability to LCAS.

Specific results are generated depending on the particular type of modification accomplished and will therefore be covered separately below.

The types of modifications possible in LCAS are:

Direct Component Modification
Insertion of Components
Copying Components
Deleting Components
Renumbering Nodes

These are in addition to the ability to add components to the component list.

The modification of a circuit does not affect a circuit file which was the source of a circuit description. Modified circuits can be saved to disk under an existing name or a new name if desired.

Direct Component Modification -

The general method of accomplishing component modification is to place the large inverse cursor on the component, value or node number to be changed and simply entering the new information. Component modification can only be accomplished on the component screen.

General considerations of changing either the component's type, specified values or nodal connections are given below.

Type - When the component type is changed the other parameters are automatically erased and must be re-entered.

Value - The value of an existing component can be changed without affecting other component entries. To change the value of a capacitor from 1uF to 2.2uF, simply place the cursor on the value cell and type 2.2u and the **[Return]** key. The new value is now entered and the circuit can be re-analyzed.

The value of a component can also be changed using the "%" and "R%" functions. For instance to increase a component's value by 12%, place the cursor on the desired component value and type -

12%

To reverse this process and return to the previous value type -

R12%

To reduce the value by 12%, type -

-12%

And again to reverse this process type -

R-12%

Node - Node numbers may be changed without affecting other component entries. Be especially careful to leave a complete circuit with all connections intact after node modifications are complete.

Node numbers must be used consecutively from 1 through the highest node number used. Node numbers cannot be skipped and all nodes must have more than one component lead connected except the circuit input and output nodes.

Node numbers are not checked for connections at entry other than to determine if they are negative or out of range. At analysis time if there are nodes with only one connection or skipped node numbers, then an error is generated.

Insertion of Components -

To insert a component into a circuit and into an existing component list simply place the cursor on the component you want to insert before. The **[Ins]** key toggles the insert mode on and off. When the insert mode is active a small "i" is displayed on the far right of the component type menu. With the insert mode active, a new component type letter entry will push down the component list by one to give room for insertion. The insert command does not change the node numbers of any existing components.

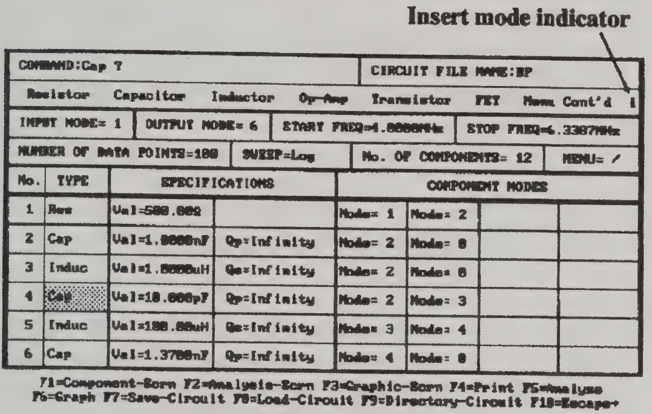
With the insertion mode "off" a new component type entry will overwrite the component listing at the cursor position. The previous component entry can be recovered at any time before all new component entries have been completed. The **[Esc]**, left arrow key and **[F10]** function key can all be used to abort the new component overwrite process. Note that the **[Esc]** and left arrow key must be used repeatedly to back over the "type" cell before the previous component is retrieved.

Sometimes it is necessary to insert a new component in series with an existing circuit between two component leads presently connected to the same node. LCAS provides an easy method of accomplishing this by using the renumber command described below in "Renumbering Nodes" to leave a gap between nodes to insert the new component. The **[Ins]** key can then be used to place the component in the proper place in the component list.

An example of component insertion is given in Figures 2-2 and 2-3 representing before and during insertion, respectively. The circuit used for this example is the "BP" circuit of Part 1's first example work session. To accomplish the insertion of a resistor into the circuit in series with the capacitor between nodes 2 and 3, the following sequence would be used.

First the insert mode is toggled on by pressing the **[Ins]** key. Note the lower case "i" at the end of the prompt/menu line in Figure 2-2.

Next the cursor is placed in the "Type" column of the line containing the component to be pushed down to make room for the insertion of the new resistor. This is the capacitor as shown in Figure 2-2.



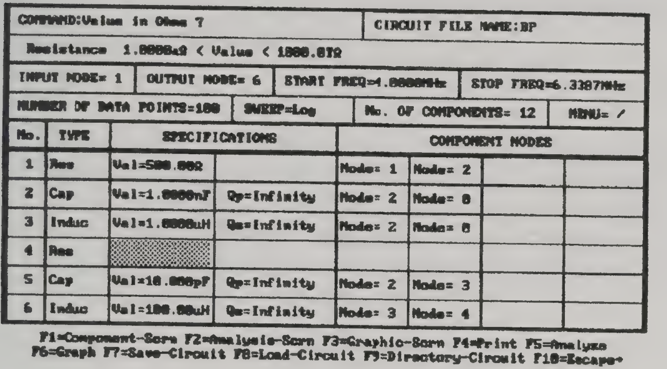
Insert mode indicator

```
COMMAND:Cap ?                                  CIRCUIT FILE NAME:BP
 Resistor  Capacitor  Inductor  Op-Amp  Transistor  FET  Menu Cont'd  i
INPUT NODE= 1  OUTPUT NODE= 6  START FREQ=4.0000MHz  STOP FREQ=6.3387MHz
NUMBER OF DATA POINTS=100  SWEEP=Log  No. OF COMPONENTS= 12  MENU= /
No.  TYPE       SPECIFICATIONS               COMPONENT NODES
 1   Res    Val=500.00Ω                  Node= 1  Node= 2
 2   Cap    Val=1.0000nF  Qp=Infinity    Node= 2  Node= 0
 3   Induc  Val=1.0000uH  Qs=Infinity    Node= 2  Node= 0
 4   Cap    Val=10.000pF  Qp=Infinity    Node= 2  Node= 3
 5   Induc  Val=100.00uH  Qs=Infinity    Node= 3  Node= 4
 6   Cap    Val=1.3700nF  Qp=Infinity    Node= 4  Node= 0
F1=Component-Scrn F2=Analysis-Scrn F3=Graphic-Scrn F4=Print F5=Analyze
F6=Graph F7=Save-Circuit F8=Load-Circuit F9=Directory-Circuit F10=Escape→
```

Figure 2-2
BP Circuit Components Before Insertion

Press the "R" key for resistor just like a standard component entry. The present state of the screen is shown in Figure 2-3.

> *Note. If the "insert" mode is not on as evidenced by the "i" indicator the procedure above will replace the capacitor with the new resistor.*



COMMAND:Value in Ohms ? | CIRCUIT FILE NAME:BP

Resistance 1.0000mΩ < Value < 1000.0TΩ

INPUT NODE= 1 | OUTPUT NODE= 6 | START FREQ=4.0000MHz | STOP FREQ=6.3387MHz

NUMBER OF DATA POINTS=100 | SWEEP=Log | No. OF COMPONENTS= 12 | MENU= /

No.	TYPE	SPECIFICATIONS		COMPONENT NODES			
1	Res	Val=500.00Ω		Node= 1	Node= 2		
2	Cap	Val=1.0000nF	Qp=Infinity	Node= 2	Node= 0		
3	Induc	Val=1.0000uH	Qs=Infinity	Node= 2	Node= 0		
4	Res	▨					
5	Cap	Val=10.000pF	Qp=Infinity	Node= 2	Node= 3		
6	Induc	Val=100.00uH	Qs=Infinity	Node= 3	Node= 4		

F1=Component-Scrn F2=Analysis-Scrn F3=Graphic-Scrn F4=Print F5=Analyze
F6=Graph F7=Save-Circuit F8=Load-Circuit F9=Directory-Circuit F10=Escape+

Figure 2-3
BP Circuit Components During Insertion

After completion of the resistor entry, the node numbers of the components from the capacitor through the last component must have 1 added to each except the ground nodes. This can be accomplished either manually or with the renumber command.

Copying Components -

In the design of a circuit it is sometimes useful to copy one or a group of components. For instance a multi-section filter is usually composed of repeated sets of the same component groups with different component values. Copying is accomplished by placing the cursor on the first component to be copied, and using the copy command -

```
/C
```

This will highlight the component the cursor is presently on. To select more than one component use the up and down arrow keys to highlight the group. When the desired components have been selected, pressing "Y" will confirm the selection and copy the highlighted components to the end of the component list. Pressing "N" will cancel the operation. Either "Y" or "N" may be lower case.

The copied components are automatically numbered beginning with the last node used. The circuit criteria cell for "Number of components" is updated to reflect the added parts.

Remember that when components are copied, other nodal numbers may have to be changed to connect these new components correctly. The input and output node may also have to be re-specified.

The highest numbered node in the existing component list is used as the lowest or starting point node number of the copied component(s).

To "Move" a group of components, first copy them to the desired location and then delete the original components. Take care to properly renumber the nodes as required.

Deleting Components -

Components are deleted by placing the cursor on the first component to be deleted, giving the slash command -

/D

This will highlight the component the cursor is presently on. To select more than one component use the up and down arrow keys to highlight the desired group. When all desired components to be deleted have been highlighted, press the "Y" key to confirm the deletion or the "N" key to cancel the operation. Either "Y" or "N" may be lower case.

Remember that when components are deleted, other nodal numbers may have to be changed to reconnect the circuit's interior components. The input and output node may also have to be re-specified.

Deleted components are removed from memory and are not recoverable unless the circuit description was previously saved to disk. It is usually easy to regenerate small circuits, but in some applications you may desire to save a circuits description to disk successively under different names to ensure recoverability.

Renumbering Nodes -

Renumbering the nodes of individual components can be manually accomplished by placing the cursor on the node to be changed and entering a new node number.

Renumbering successive components nodes is easily accomplished in LCAS by locating the cursor on the first component to be renumbered, and giving the slash command -

/R

This will highlight the component the cursor is presently on. To select more than one component use the up and down arrow keys to highlight the desired group. When all desired components to be renumbered have been highlighted, press the "Y" key to confirm the selection or the "N" key to cancel the operation. Either "Y" or "N" may be lower case.

Next, in response to the prompt, specify the increment to add to the existing node connection numbers. The increment entry can be positive or negative.

Renumbering does not affect node 0 (ground) connections.

Note !
If a negative increment is specified and that increment will make a node number less than or equal to 0, it will be made 0. The 0 node is the ground and may have be changed to the proper nodal connection point.

ANALYSIS CRITERIA

The specification of the analysis criteria tells LCAS the basics of how the circuit is to be analyzed. Each of the required entries in the "circuit criteria" section of the screen is discussed below. Changes to the circuit criteria may be accomplished in either the component or analysis screen.

All entry or modification to values in the Circuit Criteria section is accomplished by placing the cursor on the appropriate "cell" and entering the new value. The existing value is shown in the command cell and will be accepted as is by pressing the **[Esc]**, **[F10]**, arrow or **[Return]** keys without entering a new value. The range of acceptable values for each entry is displayed in the menu/prompt line.

Entries outside of the displayed range will cause a "beep" and rejection of the value. A proper entry is accepted and placed in the cell after pressing one of the cursor control arrow keys or the **[Return]** key.

Input Node - Specify in this cell the node to be used for the input circuit excitation. The circuit excitation is a 1 volt root-mean-square sinusoidal signal, with a zero ohm output impedance. Also see the preceding Part 1 on "Inputs, Outputs, Sources and Terminations.

Output Node - Specify in this cell the node at which the output response is to be read. The specification of a node as output presents no loading to the circuit. Also see the preceding Part 1 on "Inputs, Outputs, Sources and Terminations.

Start Frequency - Specify in this cell the frequency in Hertz that the analysis is to begin on. All the standard engineering and scientific multipliers are applicable. The start frequency is the first point that is analyzed, so include it as

one point when determining the desired number of data points, below.

The start frequency cannot be greater than the stop frequency.

Stop Frequency - Specify in this cell the frequency in Hertz that the analysis is to end on. All the standard engineering and scientific multipliers are applicable. The start frequency is the last point that is analyzed, so include it as one point when determining the desired number of data points, below.

The stop frequency cannot be less than the start frequency. The stop frequency can be the same as the start frequency if only one data point is specified.

Number of Data Points - Specify in this cell the desired number of data points in the range of 1 to 300. If only one point is specified it will be at the stop frequency. If two are specified, one will be at the start and one at the stop frequency. Inputs outside the range of 1 to 300 will not be accepted.

The number of data points is not the same as, but is 1 greater than, the increment of the frequency steps desired divided into the difference between the start and stop frequency. For example to get 10 even steps of 1 MHz each when analyzing with linear steps from 10 to 20 MHz, use 11 data points. 10 data points would only result in 9 increments of analysis and an odd frequency step size.

See the "Selection Criteria" at the end of this section for more information on choosing the number of data points.

Sweep Mode - LCAS provides both linear and logarithmic sweep modes. Many engineers prefer to use the logarithmic mode when analyzing over frequency ranges greater than one decade. Place the cursor on the sweep cell and enter either "L" for linear or "N" for non-linear (logarithmic) sweep.

The sweep mode selection made for analysis purposes also effects the graphing function, described later. Selecting the linear mode results in frequency steps which are determined by the formula:

$$\text{freq. increment} = \frac{\text{stop - start freq.}}{\text{number of data points -1}}$$

The resulting frequency increment is added to the last frequency analyzed at each of the data points, beginning with the start frequency.

Selecting the logarithmic mode results in frequency steps which are logarithmic and determined by the formula:

$$\text{freq. multiplier} = 10^{\left(\frac{\log_{10}\text{(stop / start freq.)}}{\text{number of data points - 1}}\right)}$$

At each new data point in the analysis a new frequency is generated by multiplying the last frequency analyzed by the frequency multiplier, beginning with the start frequency.

Selection Criteria

You should consider several factors when choosing the frequency increment, sweep method and number of data points for a circuit. Many engineers prefer to use linear increments for frequency ranges less than approximately 1 octave, and logarithmic increments for ranges greater than 1 octave. Multi-decade frequency ranges are almost always viewed against a logarithmic frequency scale.

Graph functions for overlaying multiple analysis information requires in most cases that the frequency increment and number of data points by the same for all sets of analysis data.

Misleading information will result if too few data points are chosen when the rate of change of a circuit's magnitude, phase or delay response is very high or changes direction. The selection of logarithmic sweep mode also increases the step size toward the stop frequency and may result in steps too far apart. Any suspicious data observed when graphing can be checked by increasing the number of data points, reducing the frequency range or performing an expanded analysis about the area of interest.

For proper functioning of the phase computations the phase difference between two data points should be less than 180 degrees. LCAS chooses the shortest path around the unit circle representing plus and minus 180 degrees of phase shift. For example in a circuit with a constantly decrementing phase angle, if one step was negative 210 degrees, the step would be interpreted as plus 150 degrees (being the shortest path) and display on the graph as a phase direction reversal.

The delay response is especially critical to the selection of the number of data points. The delay is calculated based on a point before and after the specific frequency of analysis, and is representative of the rate of change of the phase vs frequency change. The points must be sufficiently close to capture the peak slope of the phase response. One indication of an inaccurate computation would be if an increase in the number of data points causes a significant change in the delay response.

Another more general indication of insufficient data points for any response would be arrived at by observing the graphed response. If peaks of any response have flat tops or sharp points then there may be a missed peak. If the graphic markers are placed successively at points about the peak of the response, and there is significant change between points, then more data points may be required to resolve it accurately.

CIRCUIT FILES

Nothing would be more tedious than to have to re-enter the component list for a circuit each time you wished to perform an analysis. LCAS provides a very straightforward and easy to use set of circuit file commands. These commands allow you to save a file to disk containing all the component parts and nodal interconnections in addition to the analysis criteria. This circuit file can later be reloaded as a complete file or merged into a new circuit description underway.

Circuit files may be kept in a separate directory or in multiple directories on different drives. LCAS uses the default drive and path chosen in the "Set-up, Default Drive, Circuit Files" command for all circuit file operations. Refer to Part 1 for specifics on setting the default drive.

The circuit file operations provided in LCAS are:

- Directory
- Saving
- Loading
- Merging
- Erasing
- Naming
- Clearing (from memory)

Each of these operations is discussed separately below.

Getting a Directory of Circuit Files

A directory of the LCAS circuit files on the current default disk drive and path (see Configuration in section 1) is given by the slash command -

```
/FD
```

or the function key **[F9]**. The directory function only selects those files on disk with the extension ".LCA". The directory is shown in two columns, each giving the circuit name, date and time of the last save. The .LCA extension is not shown. If the component screen is not currently active, then it is switched to prior to the display of the circuit directory. The circuit directory overlays the component screen, and is removed by pressing either the space bar, **[Esc]** or the function key **[F10]**.

Performing a directory of circuit files returns to the "Files" command prompt -

```
Directory Save Load Merge Erase Name Clear <Files Cont'd>
```

while leaving the directory displayed. The prompt "Files Continued" is only present if more files were located on the drive/path than could be displayed.

The directory listing can hold 30 files on one screen. If the number of circuit files is more than one full screen then the menu prompt will have the words "<Files Continue>" displayed at the end, indicating that more file names are available. Pressing the "F" key will scroll the display to the next page. To view the first page again the **[F9]** or "D" key is required. The present displayed screen of circuit files can be held and any of the "Files" commands entered by simply pressing the key for the desired command. See the section below on File Functions from the Directory for more information.

If no files with the extension ".LCA" are found on the current default drive, then the message "**NO FILES FOUND!!!**" is displayed. If the drive door is not closed, the disk is unformatted or no disk is present then the message "**DRIVE NOT READY!!!**" is displayed. In either case, correct the problem and repeat the command.

LCAS will perform a directory of files on the circuit files default drive and path. To select another drive or path, change the default using the set-up drive slash command -

/SDC

It is often useful to separate groupings of circuit files into directories for maintenance of projects, customers, etc. or just to separate types of circuits.

File Functions from the Directory

When the directory is completed, or any page of a multi-page display is shown, the menu prompt returns to the "Files" command menu and allows you to execute or continue with file functions while the directory remains displayed.

Selecting the "Load" or "Merge" function at that time leaves the present page of the directory displayed and places a highlight cursor on the first file listed. The cursor can be positioned over the desired file to load (or merge) by using the cursor control keys. The file is then loaded (or merged) using the **[Return]** only.

The Save, Erase, Name and Clear functions also leave the directory displayed which is useful in checking spelling or determining the names of related files. These functions do not allow the selection of a file with the cursor, however.

Saving Circuit Files To Disk

Once a circuit is described it should be immediately saved on diskette to avoid inadvertently losing the information. Even if the circuit description is not completed, it is a good idea to save the circuit description occasionally, especially for large circuits. Circuit descriptions are saved with the slash command -

/FS

or the function key **[F7]**. When LCAS asks for the file name, a name of 8 characters or less should be given followed by the **[Return]** key. The standard DOS file name rules apply to the circuit file name. No extension should be given as LCAS always supplies the extension ".LCA" to allow it to recognize circuit files on disk.

If the circuit has been previously named or saved or was originally loaded from a circuit file then a name is already assigned to the circuit. That name will be shown in the "Circuit File Name" cell in the upper left of the display screen. To accept that name for saving the circuit, just press **[Return]**. To save the circuit under a different name and update the Circuit File Name cell accordingly, type in a new file name and press **[Return]**.

LCAS saves all the information entered into the circuit criteria section of the display screen as well as the component description. This saves having to remember and repeat the normal criteria for analysis of a given circuit. To use this feature, a circuit description should be saved a final time when all the criteria and component descriptions are finalized.

LCAS normally saves circuit files to the circuit files default drive and path. To save a file to another drive, simply add the drive designator to the file name when prompted as in -

A:filename or B:filename

Alternately, change the default drive and path using the Set-up Default drive slash command -

/SDC

If a file by the same name already exists on the disk, then LCAS will request confirmation to overwrite the existing file with the new information. If the diskette has insufficient room to store the file then the message "**DISK FULL!!!**" is displayed. At that time replace the diskette with one containing enough room and repeat the command, or erase old or unused circuit files using the slash command -

/FE

If the drive door is not closed or no formatted disk is present in the drive then the message "**DRIVE NOT READY!!!**" is displayed. In either case, correct the problem and repeat the command.

Saving a file to disk does not change or erase the information in memory. The form of the information saved to disk is given in the appendices.

The directory command or [F9] can be used to display a list of the files presently in the designated drive and path during the circuit saving process. This feature is handy when checking spelling or the names of related files.

Loading Circuit Files From Disk

Previously saved circuit files can be loaded into LCAS with the slash command -

/FL

or the function key **[F8]**, followed by the name of the file to load.

Simplified Load Procedure

LCAS provides a simplified load procedure where the file name does not have to be typed in. First get a directory of the circuit files using the -

/FD

or

[F9]

command. If there are more files than will fit on one screen then use the "F" key for the "files continued" function if necessary to display the desired filename. The "Files" menu prompt will remain on the screen allowing you to enter the load command -

L

which will present a highlighted cursor over the first file name in the file directory listing. Place the cursor over the desired file name to load using the cursor control keys and press **[Return]** to load that file.

LCAS will load files from the default drive and path selected in the set-up configuration under "Default Drive, Circuit Files". To

load a file from another drive, simply add the drive designator to the file name when prompted as in -

A:filename **or B:filename**

You cannot use the simplified load procedure when specifying a different drive by this method. Alternately, change the default drive and path using the Set-up Default drive slash command -

/SDC

and then use the -

[F9] L

loading option.

When LCAS loads a new circuit file, the circuit listing presently in memory will be cleared.

If no circuit with the name given is found on the disk then LCAS will return with the display "**FILE NOT FOUND!!!**". It is probably best at this point to perform a directory of the diskette to make sure the desired file is on the disk and the filename spelling is correct.

If the drive door is not closed or no formatted disk is present in the drive then the message "**DRIVE NOT READY!!!**" is displayed. In either case, correct the problem and repeat the command.

Merging Circuit Files

The ability to merge circuit files is a very powerful feature that allows common circuit "modules" to be kept on disk and used repeatedly in new circuits. These "supercomponents" are the equivalent of a set of software "macros" available for common software functions.

Merging provides the capability to design a large circuit as several small functional blocks. Thus each block can be analyzed in detail alone, probably faster than the larger circuit. Later, the individual blocks can be merged into the entire circuit and the overall operation examined.

Merging also gives you the ability to design common test and analysis tools, then, pull them temporarily into a circuit to determine some specific aspect of its operation and later discard.

A file is merged into an ongoing circuit definition by placing the components from the circuit file at the end of the component list. The merged components have node numbers in the same sequence as the circuit when it was saved to disk, but are numbered beginning with the last node number in the present component list before the merge. The merged file does not change the circuit criteria section of the present circuit other than updating the output node. The easiest way to merge a circuit without too much node re-numbering is to merge circuits files at the point where they belong in the circuit instead of waiting until all other components are defined.

A circuit file is merged into a component list with the slash command -

```
/FM
```

and responding with the name of the circuit file to merge.

LCAS will merge files from the default drive and path. To merge a file from another drive, simply add the drive designator to the file name when prompted as in -

A:filename or B:filename

Alternately, change the default drive and path using the set-up default drive slash command -

/SDC

LCAS provides a simplified merge procedure where the file name does not have to be typed in. First get a directory of the circuit files using the -

/FD

or

[F9]

command. If there are more files than will fit on one screen then use the "F" key for the "files continued" function if necessary to display the desired filename. The "Files" menu prompt will remain on the screen allowing you to enter the merge command-

M

which will present a highlighted cursor over the first file name in the file directory listing. Place the cursor over the desired file name to merge using the cursor control keys and press **[Return]** to merge that file.

There must be components presently defined in the editor before a circuit file can be merged. If the component list is presently clear then the error message "NO COMPONENTS TO MERGE !!!" is displayed in the menu/prompt line.

Erasing Disk Files

Circuit files may be erased on the circuit files default drive and path using the slash command -

/FE

and giving the name of the file to erase at the prompt. An erased circuit file cannot be retrieved. The wildcard character "?" can be used to specify groups of files to be erased. For instance if you had successively saved files by the name "CIRCUIT1", "CIRCUIT2", etc., they could all be erased by specifying the name

CIRCUIT?

LCAS will only erase files on the circuit files default drive and path. To erase a file on another drive, simply add the drive designator to the file name when prompted as in -

A:filename or B:filename

Alternately, change the default drive and path using the set-up default drive slash command -

/SDC

The directory command or [F9] can be used to display a list of the files presently in the circuit files default drive and path during the circuit erasing process. The use of the highlighted cursor to select files for deletion is not provided for safety. This feature is handy when checking spelling or the names of related files.

Circuit files or any other disk files may also be erased using DOS. LCAS keeps no separate record of files which would be harmed by erasing from DOS.

Naming Circuit Files

When a circuit is saved to disk, LCAS asks for a name to assign to the circuit file. It is often convenient to be able to name circuit files before or without saving to disk, or to change the name of a circuit loaded from disk. This allows applying specific names for outputting data to a printer. A circuit in memory is named using the slash command -

```
/FN
```

and supplying the new name at the prompt.

An example of the use of the name command might be the successive naming of a circuit Test1, Test2, Test3 etc. as the circuit parameters are changed and a new graph is produced and printed. Thus each printout is supplied with a different name for ease of identification later.

The option to change the name of a circuit file in memory is offered each time the circuit is saved to disk using the file save command. Therefore the file name command is not required before saving a circuit under a different name.

The directory command or [F9] can be used to display a list of the files presently in the circuit files default drive and path during the circuit naming process. This feature is handy when checking spelling or the names of related files.

Clearing A Circuit File In Memory

The present circuit description including the component list and circuit criteria can be erased from memory using the slash command -

```
/FCY
```

where the "Y" represents the yes response to the safety prompt requiring confirmation before clearing the memory.

Once erased the circuit description is gone forever from memory. The file clear command does not affect any files on diskette.

CIRCUIT ANALYSIS

The analysis of a linear circuit is the central core of LCAS' functions. The component and circuit entry, editing and file handling capabilities make it easy to create circuits for LCAS to analyze. The output and graphic capabilities use the analysis results to produce easily interpreted data. Because of this, special emphasis has been placed on making the analysis function both fast and error free. Most of the analysis routines in LCAS are written in assembly language for speed, and uses special routines to maintain the required accuracy beyond the capability of most compiled languages.

The installation of a Numeric Data Co-processor (8087 or 80287/80387) in your computer will increase the speed of analysis by 5 to 10 times. If you have a Numeric Data Co-processor installed, LCAS must be made aware of it before it is used. Refer to the configuration section in Part 1 for more details.

Analysis of a circuit requires that the circuit analysis criteria section be completed. A beep and momentary prompt of "**BAD ENTRY!!!**" will result if one of the analysis criteria elements is incorrect. LCAS will place the cursor on the criteria cell that appears to be incorrect.

Initiating the circuit analysis is accomplished by using the slash command -

```
/A
```

The **[F5]** function key can alternately be used. Both commands are identical and result in immediate analysis, unless the circuit has already been graphed and the graphic markers set for an expanded analysis. See the Expanded Analysis section below for more information.

When analysis has been initiated, the display is switched to the "Analysis Screen". The top portion of the analysis display screen is the same as the component screen, but the component list is replaced by the tabular printout of the analysis results.

Analysis will continue until all points between and including the start and stop frequencies have been analyzed.

The analysis process may be terminated at any time before completion by pressing any key. Terminating the analysis does not invalidate any of the completed data. If a graph of the terminated analysis data is requested, the stop frequency for the graph is chosen at the last completed step.

The analysis proceeds at a rate determined by the number of nodes in the circuit, and is independent of the number of components placed between those nodes. If you are curious enough to time some analysis, you may notice differences between certain circuits with the same number of nodes. That is because some components add "internal nodes" to the circuit during calculation. For instance a capacitor that has been given a series loss Q factor that is finite has an internal node added to connect the series resistor used to simulate its Q. Components which add internal nodes are:

Capacitors with finite Q specified as series loss

Inductors with finite Q specified as series loss

Transformers

Loop Amplifiers

VCOs

÷ N, with a non-zero delay specified

Delay Lines

Each of these components adds one internal node during the analysis computation except the Loop Amplifier which adds two nodes. The added internal nodes reduces the maximum number of nodes allowed from the limit of 64, but do not reduce the maximum number of components from the 128 limit.

The analysis results are printed in four columns giving the magnitude and phase response of the defined circuit versus frequency. The magnitude is given in linear (volts RMS) and logarithmic (decibels relative to 1 volt RMS) format. The phase angle is given in degrees relative to the input. Any of the data may have engineering multipliers applied and will be displayed with the letter designation as appropriate. This gives much greater accuracy for both very small and very large numbers. Do not be surprised to see mdB for milli-deciBels as well as the more common kilo- and Mega-Hertz.

When the analysis is completed, the results may be scrolled through using the cursor control keys. One line of the analysis results is highlighted. The up and down arrow keys move the highlighted results up and down one item at a time. The **[PgUp]** and **[PgDn]** keys move up and down one page at a time, and the **[Home]** and **[End]** keys move to the first and last result, respectively.

The **[F1]** function key can be used to change to the component screen and the **[F2]** function key used to return to the analysis results screen.

Errors in the Analysis Process

There are two types of errors that can occur during analysis. The first is an error in the circuit description that LCAS can determine and report. The second is an under or over-flow in computation. An under or over-flow can also result from an error in the circuit description such as an incomplete path from the input to output node.

Errors which are trapped and reported at analysis time include:

- A node with only one component lead connected. (except the input and output nodes)

- Non-consecutive node numbers which skip one or more node numbers.

Under and over-flow errors are caused by insufficient precision or dynamic range in intermediate calculations. These errors are displayed during the analysis process by use of the plus or minus infinity instead of a value output for the response at one or more data points. Under or over-flow can occur in the magnitude response and the phase response still remain accurate due to the difference in calculation method used for these two values.

It is very rare for there to be an under or over-flow error when using the 8087/80287 co-processor in a correctly entered circuit. If this does occur it is likely caused by a circuit connection or value error.

Under or over-flow is more likely to occur when not using a co-processor. This is because of the reduced dynamic range without the co-processor. It is difficult to determine in advance if a circuit will suffer from under or over-flow calculation errors. The "FWD_TRAN.LCA" circuit file on the master diskette is an example of a file which will not analyze properly without the 8087.

Suggestions for solution to under and over-flow problems are given in the Problem Locator, Appendix J.

Expanded Circuit Analysis

An analysis is normally performed strictly according to the criteria defined in the top of the component or analysis screen. After graphing the analysis results you may want a more detailed or "expanded" analysis of a portion of the frequency range displayed on the graph. This allows analysis of interesting details of the response.

Expanded analysis requires the use of the graphic screen, so a review of the graphic section may be required before the following explanation will be meaningful.

To accomplish an expanded analysis, the graphic markers are used to bound the frequency range of interest on the graph. Graphic marker 1 may be used alone to set a new upper frequency limit, or marker 2 alone to set a new lower frequency limit, or both markers may be used to bound the start and stop frequencies desired (see the graphic section for more detail on using the graphic markers). Next request an analysis using the slash command -

```
/A
```

The [F5] function key will *not* work to perform an expanded analysis, but will instead perform a regular analysis. The prompt line of the screen will present a new menu, displaying:

```
Analyze   Expanded Analysis
```

Select the "E" option for Expanded Analysis and a new analysis will be performed using the graphic marker derived start and stop frequencies.

The expanded analysis results may now be graphed or output to printer or file just as any other analysis. An easy way to return to the full analysis range is to strike the **[F5]** function key.

Note that when performing an expanded analysis, the frequency used for Q calculation remains unaffected, in other words the Q determining resistors are calculated as if the normal start and stop frequencies are unchanged.

GRAPHICS

Introduction

In the case of engineering data, a picture is truly worth a thousand words. LCAS' facility with graphing analysis results make it a pleasure to use. If you do not have a color/graphic or EGA adapter, you are missing an important part of LCAS' functionality. LCAS can make new graphs from data, and overlay, add and subtract other data onto an existing graph. Each of these subjects is covered in more detail below.

Section Layout

LCAS includes extensive graphics options and variations. Because of the many possible variations in graphing data, this section begins with a layout of how the remainder of the graphics topics are organized.

GRAPHICS

Introduction

- Section Layout
- The Graph Menu
- Initial and Subsequent Graphs
- The Graph Screen
- Graph Data Sources and Routes

Graph Options

- Setting the Graph Scale Mode
- Graphic Markers
- Plotting Delay Response
- Noise Power Display
- Area Under the Curve
- Phase Jitter Calculation

New Graph

- Addition and Subtraction
- Present Only

Overlay Graph

- Addition and Subtraction
- Present Only

Graph Data File

- Loading the Data File
- Menu Options
- About Data Files

The Graph Menu

Graph functions in LCAS are accessed through the Graph menu, obtained by giving the slash command -

```
/G
```

If the graphic command is given when there are no analysis results present then LCAS assumes that you desire to graph data saved in a file, and will go directly to the menu prompt for loading a data file. This case is covered more explicitly later and will not be considered here.

The graph slash command will result in one of two slightly different menus. If there has been no previous graph generated in this session since starting LCAS then the available prompt is:

```
View Graph   Graph Data File   Set Scale Mode
```

The three options allow generation of the graph immediately, selected by the "V" option, or generation of a graph from data previously saved to disk file selected by "G", or setting of the scale mode selected by "S".

If a graph has been previously generated and displayed on the graphic screen and the present analysis results use the same sweep mode (Log or Lin), then the menu presented is:

```
New Graph   Overlay Graph   Graph Data File  Set Scale Mode
```

allowing the added options of combining the previous graph information with the new information either in a New graph or an Overlay graph. The option to generate a completely new graph without regard to any previous graph scale information is allowed within the New Graph option.

Initial and Subsequent Graphs

Graphing data naturally requires that an analysis was previously performed to generate the data. The first graph generated will result from the slash command -

```
/GV
```

for Graph, View Graph, or the [F6] function key. In just a few seconds the graph will be displayed. If no graphics adapter is installed then the message "NO GRAPHICS ADAPTER !!!" is displayed.

If there is no analysis results presently in memory then LCAS assumes you want to graph the results of a previous analysis and switches to the prompt for graphing a data file. See the section on "Graph Data Files" below.

After the initial graph is present on the graphic screen, several new options become available for graphing new data with the same sweep mode (Log or Lin). This is represented by the new prompt line after the /G command -

```
New Graph   Overlay Graph   Graph Data File  Set Scale Mode
```

A completely new graph is generated by the slash command -

```
/GNP
```

for Graph, New, Present only. The [F6] function key is the equivalent command and will always draw a new graph from the data in the analysis screen if available. If there is no analysis data available then [F6] will go to the Graph Data File prompt.

The commands to add or subtract in either New or Overlay mode are discussed later, but first the graphic screen and the basic graphic options available with any graph are discussed.

The Graphics Screen

When a graph is generated, LCAS will switch to the graphics screen to display the graph, removing the text screen used for prompts unless you are using both a monochrome and color/graphics adaptor. Figure 2-4 below shows a typical graphic screen. The graph is shown on a blue background with the circuit name displayed at the top center of the screen Both magnitude (in dB) and phase response are displayed. The magnitude uses the left vertical scale in white, while the phase uses the right vertical scale in magenta color.

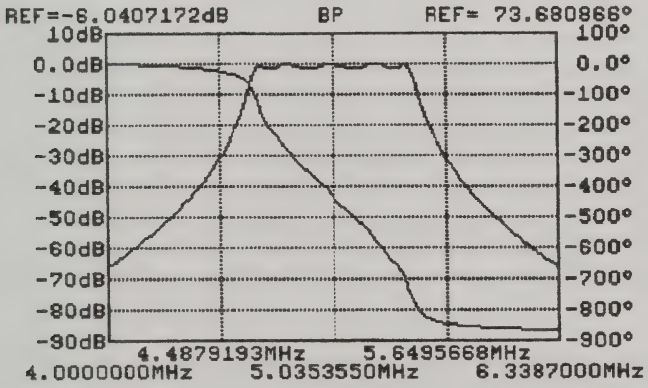


Figure 2-4
Typical Magnitude / Phase Graph Screen

Both magnitude and phase responses are shown relative to a reference. The peak level of both sets of data are always represented at 0 dB and 0 Degrees. The absolute reference for each is given at the top of the screen in matching color unless the manual scale mode was used.

Graph Data Sources and Routes

After the initial graph is displayed, new analysis data may be generated from altered circuit connections, component modifications or from entirely different circuits. LCAS offers two options for graphing this new data, besides generating an all new graph. First, the new data may be used to add or subtract from the data used in the original graph. Second, the new data may be presented as a graphic overlay on the original, either new, added or subtracted from the original. These two options are called "New" graph and "Overlay" graph.

For any of these techniques to be of much use, the newly generated analysis data should correspond with the original in frequency range and number of data points. Although this restriction is not absolutely necessary in overlays of new data, adding or subtracting data requires identical number of data points and sweep mode. If the data points are not the same then addition and subtraction are not provided. If the frequency range is not the same then the message "FREQUENCY NOT SCALE" is substituted for the frequency scale on the graphic screen.

Overlays are not allowed of data taken at different frequency scale increment modes. That is both must be at either linear or logarithmic increments.

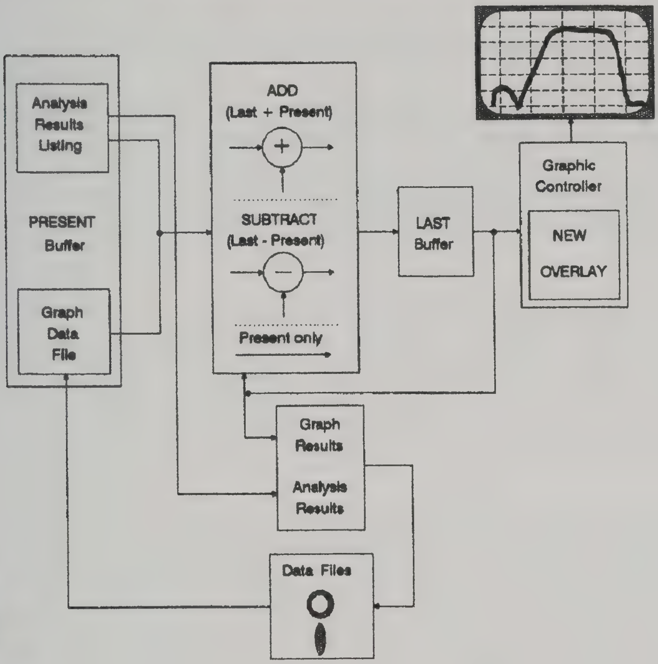

Analysis
Results
Listing
PRESENT
Buffer
Graph
Data
File
ADD
(Last + Present)
+
SUBTRACT
(Last - Present)
−
Present only
LAST
Buffer
Graphic
Controller
NEW
OVERLAY
Graph
Results
Analysis
Results
Data Files

Figure 2-5
Graph Data Sources and Routes

Figure 2-5 shows a representation of the three locations that numerical data can be taken from to generate graphs. They are:

1. The Analysis results screen, referred to as the "present" data.
2. A Data file which holds data saved from a previous analysis result, or from another program.
3. The Last Graphed data buffer which holds the data from the last graph plotted, referred to as the "last" data. This data can be used to add or subtract either the "present" data and/or data from for a Data file.

Some typical methods of using this capability are to:

1. Show the sum response of two or more circuits over the same frequency range. In LCAS, a large circuit can be split into smaller functional modules, with each module analyzed separately. The larger circuit's overall response can be seen by adding each modules response together, forming the overall response.

2. Show the effect of changing a component or value. For instance, the incremental effect of a component change can be shown by a subtraction of response after the component change from the initial response. While an overlay of the before data with the changed data will show the two response curves together.

3. The subtraction or difference graphing can be used very effectively to compare two related outputs of the same circuit. For instance, a quadrature splitter having two outputs of the same amplitude but 90 degrees out of phase can be analyzed once on one output and graphed. Then the output node is changed and the analysis results subtracted to display the exact amplitude and phase relationship between the two.

4. Graph data files of previous responses indicating desired performance can be overlayed on a graph for comparison purposes. Graph data files can even be manually generated which present a "mask" of acceptable performance limits.

Graphic Options

Several options may be used to change the graphic display initially generated by LCAS while the graphic screen is active.

Setting the Graph Scale Mode

LCAS is set to operate with automatically generated vertical scales by default. An alternate manual scale mode can be set and will be maintained until changed back to automatic or until the program is quit. The manual scale mode is set with the slash command -

/GSM

for Graph, Set Scale Mode, Manual. To return to automatic scale mode the command -

/GSA

is used standing for Graph, Set Scale Mode, Automatic.

Whenever in the manual scale mode, LCAS will prompt for the maximum and minimum scale values to use just before generating a graph. The prompt allows you to chose which response(s) are to have their scales manually set. Those not specifically chosen and set are automatically computed.

Once the proper entries are made the "View Graph" option in the graph menu is used to generate the graph.

If a graph overlay is selected then the option to set the scales is not offered since the overlay must use the same scales as the original graph.

Plotting Delay Response

Pressing the "D" key while viewing a graph in the graphic screen will exchange a plot of group delay versus frequency for the phase response. The group delay times are shown on the right vertical axis. Pressing the "P" key will return to the original phase response plot. The delay response is referenced to an absolute group delay shown at the top of the screen, and shown with the peak at 0.0 relative time delay on the graph, when automatic scale mode is active.

LCAS calculates the group delay information, after the "D" key is pressed, from the phase data computed during the analysis process. Thus even if the graph is generated from a data file which contains no delay information, LCAS will still generate this response.

Graphic Markers

Two vertical line "Markers" are available to pinpoint any location on the graph. Marker #1 is active when the graph is first displayed, but is not visible because it is at the edge of the screen. Use the left or right arrow keys to bring it onto the graph, and the response levels at it's present location will be displayed at the bottom of the screen. The 2nd marker is made active by pressing the "2" key. The "1" key will return control to the 1st marker. To remove a marker and its information line at the screen bottom, place the marker off the screen using the **[Home]** or **[End]** keys.

The first marker shown in white is normally associated with the magnitude response curve, and the second in magenta is associated with the phase or delay plot. When the first marker is active, pressing the up arrow cursor key will cause the marker to seek the maximum level on the magnitude response, while the

down arrow key will seek the minimum level. Likewise when the second marker is active, the up arrow seeks the maximum and the down arrow the minimum of the phase or delay plot. Reminders of these actions are given on the monochrome screen if both adapters are available.

The graphic markers can be used in several different ways:

- Pointers to determine the level at any point on the graph.

- Marker 1 and marker 2 can be set to bound the frequency limits of an expanded analysis. For instance to get a more detailed view of the peak of a filter's response, the markers are placed at the 1 dB points on either side of the peak. Then the slash command -

  /AE

  is given, resulting in an analysis between the two markers. When these results are graphed, the view is "expanded".

- Marker 1 and marker 2 can be set to bound the frequency limits for an integration of the magnitude response power output. After the markers are placed the computation is performed by pressing the "**A**" key. This effectively calculates the "area under the curve" assuming there is 1 Watt per Hertz input to the circuit.

Noise Power Display

The noise power represented by the area under the magnitude response can be displayed by pressing the "N" key. The display added to the bottom of the screen will include three items:

1. The input power per Hertz to the circuit input node "P_{in}", always 1 watt per Hz.

2. The total power output "**Pout**" represented by the area under the response curve at the circuit output node. This is an integral of the power represented by the frequency response.

3. The last figure given as "**Pout - MKR1**" is the total power represented by the response minus the level at marker 1. By placing marker 1 at the proper spot and pressing the "N" key, the normalized noise power is displayed. For instance, if a bandpass filter is displayed on the graph, with a source and terminating impedance of 50Ω, the resulting output power will be 6 dB low due to the loss in these impedances. By placing marker 1 in the filter passband, assumed to be at -6 db absolute, then the resulting noise power minus marker 1 will be 6 dB greater, or four times the noise power. In other words, the noise power given is the noise power output relative to an imaginary 0 dB gain point at the cursor location.

Moving either of the markers or pressing any key on the keyboard will remove the noise data. If marker 2 was on the screen when the "N" key is pressed, its data is replaced by the noise power data. Pressing any key will return the marker 2 data.

The normalized noise power output may be one of the more difficult points in LCAS to grasp. Try the sample bandpass filter circuit, "BP" with marker 1 to satisfy yourself of the validity of the generated information.

Note, when normalized, the value in watts directly represents the noise BW in Hz. Hence if Pout - MKR1 = 10kW, then the noise BW is 10kHz. This capability is especially useful in PLL and filter circuits.

Area Under the Curve

A variant of the noise power display can be used to find the power in a certain portion of the graph response. This function

integrates the magnitude response between two points set on the graphic screen using the two line graphic markers. There are 3 methods of setting the two points between which the power is computed:

1. If only Marker 1 is visible on the screen, the frequency range is taken from the normal start frequency up to the Marker 1 set point frequency as displayed at the bottom of the graph.
2. If only Marker 2 is visible on the screen, the frequency range is taken from the Marker 2 set point frequency as displayed at the bottom of the graph up to the normal stop frequency.
3. If both markers are visible on the screen, the frequency range is from the lower marker to the upper marker. It does not matter what order the markers are set.

If neither marker is on the screen then the Area function is like the Noise power function, with the addition of the power in dBW.

When the two graphic markers have been set to bound the frequencies of interest, pressing the "A" key computes the absolute power represented by the magnitude response between the two markers. The results are displayed on the bottom line of the graph screen.

The power is computed in the same manner as the "Pout" function of the noise power display. That is the power shown is the output power of the portion of the response bounded by the markers relative to a circuit input power density of 1 Watt per Hertz.

The power output is presented both in Watts and in dBW.

Power Ratio Determination

By bounding first one area of the graph and computing power, and then a second area, the relative magnitudes or ratio of the

two powers can be easily determined. The ratio between the two magnitudes can be determined in dB by directly subtracting the two dBW figures computed.

As an example of the use of the Area function, consider a filter response which has a slight "bump" in level in the stop band and you wished to know how much power this represented with respect to the passband.

Phase Jitter Calculation

LCAS includes the capability to calculate the phase jitter represented by the single-sided noise energy on a carrier. This applies to the noise sidebands calculated by LCAS when modeling PLL circuits only. Refer to Appendix D for an example of measuring phase jitter in PLLs.

When a graph is displayed the graphic line markers are used to bound the frequency range of interest, and the "A" key (area function) used calculate the energy represented by the magnitude response in this frequency range. Alterately the noise power function can be used to calculate the noise power over the entire displayed frequency range. After calculation of the sideband noise energy, strike the "J" key and energy values will be replaced by the equivalent phase jitter in both degrees RMS and radians RMS.

The phase jitter measurement is used mainly in telecommunications to determine the effect of noise on typical digital signals, which can tolerate only a certain amount of phase jitter. Telecommunications links are commonly measured in peak to peak phase jitter. If the peak to peak value is required then simply multiply the displayed RMS results by 5.15. Telecommunications links are also typically measured for phase jitter in the 4 to 300 Hz and the 20 to 300 Hz ranges.

New Graph - Addition and Subtraction

The purpose of the New Graph function is to erase the old graph and generate a totally new graphic screen.

After the initial graph is displayed the new graph slash command -

```
/GN
```

results in the prompt line

```
Add (Last + Present)   Subtract (Last-Present)   Present only
```

Where "last" refers to the analysis data last used to prepare a graph, and "present" refers to the analysis data presently in the analysis screen, or coming from a data file. See Figure 2-5 for a pictorial representation of the sources and routes of graphs. The addition and subtraction of graphs require that the original and graph data to be added or subtracted share the same frequency scale mode. That is both must be either linear or logarithmic. Both sets of data must also have the same number of data points. If the frequency ranges do not match then the message "FREQUENCY NOT SCALE" is substituted for the frequency scale on the graphic screen.

The graph scales are regenerated for any of the new graph options, either automatically or manually, based on the current scale mode setting.

Add

If the Add option is selected then the analysis data presently in the analysis screen is added to the data used to generate the last graph at each coincident data increment point. The new resul-

tant data is then used to prepare a new graph, erasing the old. Immediately following an Add with a Subtract will cancel or "undo" the effect.

Subtract

If the Subtract option is selected then the analysis data presently in the analysis screen is subtracted from the data used to generate the last graph at each coincident data increment point. The new resultant data is then used to prepare a new graph, erasing the old. Immediately following a Subtract with an Add will cancel or "undo" the effect.

Present Only

The Present Only option is used here to generate a totally new graph based on the present analysis screen only, or data from a data file only.

Note that the data in the analysis screen does not change with the add, subtract or present only command. It is always assumed to be the "present" data with the "last" held in a separate buffer used to generate the graph.

Overlay Graph - Addition and Subtraction

Graphs may be overlayed in LCAS as if each were on a piece of clear film. When overlaying graphs only the data fitting into the magnitude and phase limits of the first graph are included. The command for overlaying a graph is -

```
/GO
```

and results in the prompt line

```
Add (Last+Present)   Subtract (Last-Present)   Present only
```

Where "last" refers to the analysis data last used to prepare a graph, and "present" refers to the analysis data presently in the analysis screen, or coming from a data file. See Figure 2-5 for a pictorial representation of the sources and routes of graphs. Overlay graphs require that the original and graph data to be overlayed share the same frequency scale mode. That is both must be either linear or logarithmic. Both sets of data must also have the same number of data points for the add and subtract options. If the frequency ranges do not match then the message "FREQUENCY NOT SCALE" is substituted for the frequency scale on the graphic screen.

Add

If the Add option is selected then the analysis data presently in the analysis screen is added to the data used to generate the last graph at each coincident frequency point. The new resultant data is then used to prepare a new graph, overlaying the old.

Subtract

If the Subtract option is selected then the analysis data presently in the analysis screen is subtracted from the data used to generate the last graph at each coincident frequency point. The new resultant data is then used to prepare a new graph, overlaying the old.

Present Only

The Present only option is used to generate a new response graph for inclusion as an overlay on the last graph. The new graph overlay is based on the present analysis results screen or data from a data file only.

Note that the data in the analysis screen does not change with the overlay command. It is always assumed to be the "present" data with the "last" held in a separate buffer used to generate the graph.

Graph Data Files

Data files are disk files of previous analysis results or data from other programs representing a frequency transfer function. They are textual information of response versus frequency that the graphic routines can use to generate and display a graph.

When a data file is loaded, its data is taken into the graph buffer called "present". Data loaded into the present buffer is treated as analysis results and can be added or subtracted from previously graphed data in the "last" buffer. See the description in "Graph Data Sources and Routes" above and the accompanying Figure 2-5 for more information on the graph buffers.

The graph data file menu option results from the slash command -

/GG

representing Graph, Graph Data File. If there are no present analysis results then only "/G" is required. At this command the graph data file menu is presented as shown below.

Directory	Load

Loading the Data File

Choosing the Load option will prompt for the file name of the desired data file.

Choosing the Directory option will present a directory of the data files on the Data Files Default drive and path. To get a directory of a different drive/path use the Set-up, Default Drive, Data Files slash command to temporarily change the default.

Use the "F" key if necessary to view "Files Continued" until the desired data file is present in the display listing. While the data file directory is displayed pressing the "L" key for "Load" will enable the simplified load procedure and place a highlighted cursor on the first data file name in the directory. Use the cursor control keys to position the cursor over the desired file name and press **[Return]** to load that data file into the "present" buffer.

Graph Menu Options

When the file data has been loaded there are two possible responses from LCAS. First, if there is no existing graph then the data file information will be loaded and the menu below is presented.

View Graph   Graph Data File   Set Scale Mode

If there is presently a graph displayed and the sweep modes of the last graph and the data file are the same, then a slightly different menu is presented:

New Graph   Overlay Graph   Set Scale Mode

Selection of either the New or Overlay options will result in the standard menu for adding new information to an existing graph if the last graph and data file contain the same number of data points. If the number of data points differ then the "Present Only" option is assumed.

Add (Last + Present)   Subtract (Last-Present)   Present only

When one of these options is selected, LCAS will compute and display the revised graph. Refer to the previous sections entitled "New Graph - Addition and Subtraction" or "Overlay Graph -

Addition and Subtraction" for more information on the actions these options produce.

About Data Files

The data file is a tabular listing of analysis results. Data files use the extension ".DAT". See Appendix G on disk file formats for more information on the data file contents. The data file is generated by LCAS when you print to a data file using the /PD slash command. The data file contents can come from either the last graphed data or the present analysis results.

This type file can also be generated by an external program or manually produced by a text editor. An example of a manually produced file might be a "mask" which can be overlayed onto specific graphs to determine if the performance data falls within set limits. Existing data in a data file can also be manually modified by using a text editor or word processor. Any such editor should always be set to the "ASCII" mode to avoid inserting extraneous codes.

Another example of using data file information is included in Appendix E on Tips and Techniques.

OUTPUTTING DATA

LCAS allows you to output the data in any of the three screens; components, analysis data and graphs. The information from these screens may be sent to either a printer or to a disk file.

The slash command -

/P

is used to retrieve the print menu. Giving the **/P** command when in the graphic screen will return to the last used text screen, either component or analysis. The print menu responds with:

```
Printer   Text File   Data File   FFT File
```

asking you to select output to the printer, or a file to be placed on disk in the format of text, data or fast fourier transform. Each of these options is discussed separately below.

Naming Output Data

Analysis, component and graph outputs all use the present circuit name for identification on the output data. To allow you to both change the name for each specific output if desired, and to supply a name for a circuit that has not yet been saved, LCAS has a "NAME" slash command -

/FN

The name command can be used repeatedly for each output. Caution should be used when changing the name. If you do not remember to return the name to its original, and then attempt to update the circuit file by saving it again, the new circuit information will be under the last given name.

The same name can be used to output the analysis, component and graphic files as a different file name extension is automatically applied to each of these. See the section on "File Extensions", below.

File Extensions

When a file is saved to disk it is given a file name extension dependent on the type information as follows:

Type	File Extension
Circuit File	.LCA
Analysis Results (Text)	.PRA
Component List	.PRC
Graphic Bit Map	.PRG
Data File (Data)	.DAT
Fast Fourier Transform	.F

Outputting to a Printer

The printer output is selected by the slash command -

```
/PP
```

which presents the following menu of options:

```
Analysis  Component  Graph
```

and is used to select whether the information is to come from the Analysis results, the Component list, or the Graph. On choosing one of these sources the transfer then begins.

Using the [F4] Print Function Key

The [F4] function key can be used from any of the three screens to send that screen's data to the printer. This is a shortcut for the slash command /PPG when in the graphic screen, or /PPA when in the analysis screen, or /PPC when in the component screen. Using the [F4] function key will not remove the graphic screen for printing.

Printer Output

The printer output is a copy of the data as presented on the screen, including the lines around the data in the component and analysis screens. The lines are formed using standard dash and "|" characters available in most printers.

The date and time of the printout is placed on any of the three screens when sent to the printer. Multiple pages of tabular listings will all have the same date and time as the first page.

When printing the graphic screen, any information currently shown on that screen will be printed. Therefore, to show the noise power data, place it on the screen by using the "N" key and press the [F4] key, or slash command /PPG.

Tested Printers

LCAS has been tested with the following dot matrix printers for both text and graphic output:

Epson MX80/100 with graphtrax, FX80/100, FX85/286, LQ 800/1000/1500, LX80

Citizen MSP 10, 15, 20, 25, 120D claim to be compatible, but not tested.

Okidata 190 and 290 series. The remainder of the Microline series of printers with "plug and play" for the IBM computer should work, but not tested.

IBM Proprinter

NEC P6 Pinwriter only tested.

Star Micronics SG10 should work but not tested.

In addition, LCAS should work with any dot matrix printer that uses the Epson graphics format.

Problems

If your printer does not work properly then perhaps the printer configuration switches are incorrectly set. If you use a daisy wheel printer or one that cannot accept LCAS graphic output, the two text screens can still be printed. Laser printers normally do not accept Epson type graphics commands.

It is also possible to save a graphic screen to a disk file and use a translator program to send the graphic information to other printers. For instance the "GRAB" program from DRHALO was used to save graphic screens from within LCAS, which were then converted for use in this manual. No translator program is included with LCAS.

If there is no printer connected to the printer port selected in the "\Set-Up, Printer, Printer Port" command, or the printer is not turned on when a printout is requested, then LCAS will beep and display the error message **"PRINTER ERROR!!!"** in the prompt area of the screen.

Text File Output

When the Print, Text File output is selected, via the command -

/PT

the next level of menu options presented for the text file output is:

```
Analysis  Component  Graph
```

and is used to select whether the information is to come from the Analysis results, the Component list, or the Graph.

Before saving the text file, LCAS first asks for a file name to use. The filename can be up to eight characters long and should not include an extension. LCAS will append its own extention based on the type of file information. The default text file drive and path will be used to save the file unless overridden by entry of a drive specification preceding the file name as in

B:filename

You can only specify a drive designation by this method. to specify a different drive and path, use the Setup, Default Drive, Text File command to temporarily change the default.

Analysis or Component Text Output

The Analysis or Component selection results in an ASCII text file. The tabular text of either components or analysis data thus saved may then be reviewed later or used by a word processor for inclusion in letters or reports. These files include the circuit criteria at the beginning of the listing. All characters as would

be sent to the printer are included in the file except page breaks and accompanying page, date and time information. The "line characters" shown on the screen are converted to dashes and bars before being sent to the file.

Graphic Bit-Map File Output

Graphic data is saved in a binary file for recall by another program. The file consists of a bit-map of the computers graphic screen video buffer beginning at B8000 Hex address, with a length of 16,000 bytes. Presently no commands within LCAS can directly use a graphic bit-map file. This capability is built into LCAS so that a separate program could retrieve graphs, for instance to give a "slide show" presentation.

If you want to import a graphic screen into a "paint" type program for manipulation or enhancement you should use that programs screen capture facility. DRHALO, PC Paintbrush and others offer such a screen capture facility.

For more information on file output formats see Appendix G.

Data File Output

Selection of the Data File response to the Print slash command -

/PD

presents the following menu:

```
Analysis  Graph
```

which is similar to the printer/text menu except the component option is deleted. The output of either of these options is raw data in ASCII form usable by other programs as input data. See Appendix G for the exact form of the data output.

The Data file output is the same as the data files used by LCAS for the "Graph Data file" slash command.

The data file can be generated from either the "present" analysis information or that used to generate the "last" graph. These sources are referred to as the present and last buffers and there relationship to the graph process can be seen in Figure 2-5 in the Graph section of this Part of the manual.

Before saving the data file, LCAS first asks for a file name to use. The filename can be up to eight characters long and should not include an extension. LCAS will append its own extention based on the type of file information. The default data file drive and path will be used to save the file unless overridden by entry of a drive specification preceding the file name as in

B:filename

You can only specify a drive designation by this method. to specify a different drive and path, use the Setup, Default Drive, Data File command to temporarily change the default.

Files of saved analysis data may be used by the graphics mode commands for graphing, adding, subtracting and overlaying with other graphed analysis. These data files may be manipulated by a text editor to simulate a specific response before re-use by LCAS. See the Graphics section for more information on this use of files. The phase locked loop jitter test in Appendix D makes use of this feature in an example.

FFT File Output

Selection of the FFT File response to the Print slash command -

/PF

presents the following menu:

Analysis	Graph

Selection of the Analysis option uses the last analyis results as the source for this output. Selection of the Graph option uses the "last" buffer containing information from the last graph displayed. These sources are referred to as the present and last buffers and there relationship to the graph process can be seen in Figure 2-5 in the Graph section of this Part of the manual.

When the FFT output of either the analysis or graph results is requested, LCAS will compute the complex rectangular coordinates of the data in the frequency domain. When generating this file LCAS extrapolates a point at DC and interpolates all other data points. This is the data that would be required by a Fast Fourier Transform (FFT) computing routine. An FFT routine requires data points in linear steps, and the number of steps must be some power of 2. LCAS will request the number of data points to compute between 16 and 2048. This output is intended for another program by DATUM Systems which performs Fast Fourier Transform functions.

Before saving the FFT file, LCAS first asks for a file name to use. The filename can be up to eight characters long and should not include an extension. LCAS will append its own extention based on the type of file information. The default FFT file drive and path will be used to save the file unless overridden by entry of a drive specification preceding the file name as in

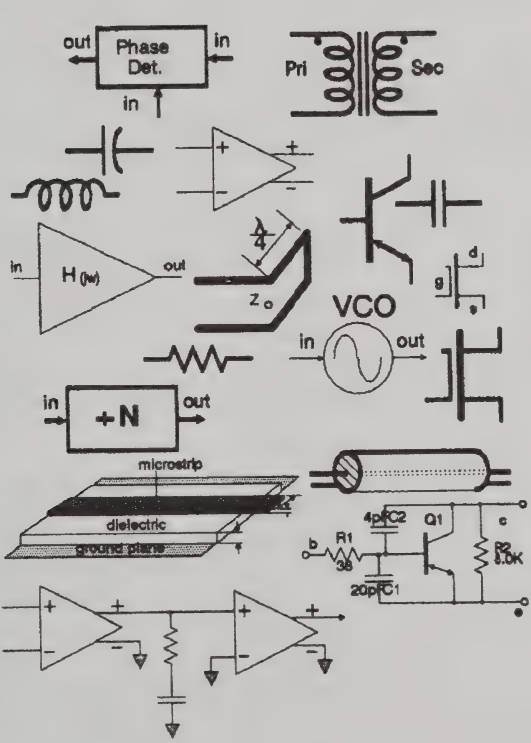
B:filename

You can only specify a drive designation by this method. to specify a different drive and path, use the Setup, Default Drive, FFT File command to temporarily change the default.

For more information on the FFT file output format see Appendix G on Disk File Formats.

PART 3 -

COMPONENT REFERENCE


out
Phase Det.
in
in
Pri
Sec
+
−
+
−
λ/4
in
H (jw)
out
Z o
VCO
in
out
d
g
s
in
+N
out
microstrip
dielectric
ground plane
4pF C2
Q1
c
b
R1
38
R2
5.0K
20pF C1
+
−
+
+
−
+
−

Introduction

This section of the LCAS manual gives detailed information about each of the components which may be entered directly into a circuit definition, including modeling information where required. Specialized modeling information for phase locked loop circuits is given in Appendix D. There are also examples of many circuit types using models in Appendix F.

Preceding the component listing is general information on component entry, modification and Q determination.

The components are listed in alphabetical order as shown below. The special T-Line and stub types are accessed by first calling the appropriate element (Transmission Line, Open Stub or Shorted Stub) and then "S" for Special.

Component	Type
Balanced Stripline	Special T-Line, O-Stub, S-Stub
Capacitor	General
Coaxial Line	Special T-Line, O-Stub, S-Stub
Delay Line	Special T-Line
Divide by N	PLL
FET	General
Loop Amplifier	PLL
Microstrip	Special T-Line, O-Stub, S-Stub
Open Stub	General
Operational Amplifier	General
Phase Detector	PLL
Shorted Stub	General
Transistor	General
T-Line (Transmission Line)	General
Voltage Controlled Oscillator (VCO)	PLL
X-former (Transformer)	General

Component Entry

Component entry is fully described in Part 2 of this manual. An abbreviated description of the entry process is given here to provide continuity with the component descriptions. Component entry assumes that you have previously generated a circuit schematic with the nodes numbered according to LCAS conventions. See Part 1 for more information on numbering nodes.

All component entry is accomplished in the "Component Screen". This screen is the first displayed when entering LCAS and after loading a circuit file.

The component menu and prompt should be visible in the prompt line (second line on the screen). If during component entry other commands have been used it may be necessary to press **[F10]** to return to the main command level showing component types in the prompt. Pressing the "**M**" key will show a second line of component types available and is used to toggle between the two prompt lines.

Starting a New Component Entry

To enter a new component the large inverse cursor is placed on the first available blank component "Type" cell at the bottom of the component listing. The cursor will go to this blank cell by pressing the **[End]** key (twice if the cursor started in the circuit criteria section). Then one of the letter keys is pressed representing the desired component as shown by the highlighted letters in the menu prompt. For instance to enter a resistor press the "**R**" key. Watch the cursor and the prompt line change to prompt for the next required entry, which in this case is the value of the resistor.

If you accidentally pressed the wrong key then back up by pressing the **[Esc]** key to "escape". The left arrow key can also be used to escape from the last entry. Any time before the completion of all entries for a component the **[Esc]** or left arrow can be used repeatedly to erase entries, i.e. to erase the last two entries press the **[Esc]** twice.

> *NOTE: The right arrow key may be substituted for the* **[Return]** *key in any cell entry. Both result in accepting the entry and moving to the next cell entry to the right.*

Value Entries

LCAS accepts component values in common *engineering* terms, or in *scientific* notation. Suppose a resistor is to have a value of 4700 ohms, or in standard engineering units 4.7k ohms. Simply enter "**4.7k**" and press the **[Return]** key to enter this value. LCAS already knows it is ohms since a resistor is being entered. You could have just as easily entered 4700 or .0047M or 4.7e3. The letter "**e**" is the scientific notation indicator and means the following number is the exponent of 10.

LCAS accepts a full range of common multiplier designators. The only point where LCAS differentiates between upper and lower case is:

A small "**m**" means milli- and a large "**M**" means Mega-.

For all designators except the letter "M", LCAS will accept either upper or lower-case entries.

The accepted list of multipliers is given below.

Letter	Name	Power of 10
a	ato	-18
f	femto	-15
p	pico	-12
n	nano	-9
u	micro	-6
m	milli	-3
none	---	0
k	kilo	3
M	Mega	6
G	Giga	9
T	Tera	12

LCAS formats each numeric input and fits it to the nearest power of 10 in factors of 3 as shown above, resulting in a mantissa between 1 and 999, using standard engineering notation. If a value is entered as ".0047M", LCAS would write the value as "4.7k".

Many values may be entered as negative numbers even though a "real" component could not normally have a negative parameter value. For instance a capacitor may have a negative value in LCAS. Frequency, time and length entries cannot be negative.

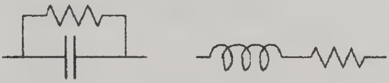
Nodal Connections

After the values and other specifications are entered LCAS will ask for the node connections. (remember that node 0 is always the ground or common connection). When all node connections have been specified, LCAS is now ready to begin another component, so it returns to the first column and awaits a command.

Component Figure of Merit or "Q"

Capacitors and inductors require a "Q" to be entered. A Q entry of 0, or no entry, results in an infinite Q (representing an ideal component). A Q value other than 0 results in the addition of a resistor to the capacitor or inductor. The resistor is placed either in series or parallel with the capacitor or inductor.

The classic low frequency Q model dictates a resistor in parallel with capacitors and in series with inductors. A high frequency Q model however, might be the opposite configuration or a combination parallel and series resistor.



Classic Low Frequency Q Models

If the Q value is entered directly then the low frequency model is chosen. If the Q value entered is preceded by a "P" or "S" then the method of connecting the Q determining resistor can be forced to a parallel (P) or series (S) configuration. Once the configuration is chosen then further changes to the component Q assume the same parallel or series connection.

LCAS shows the present connection of the Q determining resistor by a "Qp=" or "Qs=" in the second specification cell for the component.

The Q determining resistor is not shown in the component list. Its value is computed at analysis time according to the part value and the frequency range of analysis. If the analysis is at linear increments then the frequency chosen for computation of Q is the analysis range midpoint or –

$$f_m = \frac{(f_{start} + f_{stop})}{2}$$

If the analysis is at logarithmic intervals then the frequency chosen for computation of Q is the geometric mean of the frequency range or –

$$f_m = \sqrt{f\,\text{start} \bullet f\,\text{stop}}$$

For capacitors the resistor is calculated by LCAS using the formulas –

$$R = \frac{Q}{2\pi f_m C}$$ Parallel resistor

$$R = \frac{1}{2\pi f_m C Q}$$ Series resistor

where f_m is the frequency calculated above.

For inductors the formulas are –

$$R = 2\pi f_m L Q$$ Parallel resistor

$$R = \frac{2\pi f_m L}{Q}$$ Series resistor

where f_m is the frequency calculated above.

LCAS uses the start and stop frequencies defined in the circuit criteria section to compute the Q resistor added to the circuit, so when an "expanded" analysis is performed, the added resistor value remains unchanged. Expanded analysis is explained further in the analysis section.

The resistors added to the inductor and capacitor described above are used to simulate the performance of real components. To properly simulate a component, especially at higher frequencies, additional parts may have to be added to the circuit in special cases. For instance at very high frequencies, inductors exhibit capacitance and capacitors and resistors exhibit inductance. When the specifications for a component do not give characteristics at high frequencies, an LCR bridge or Q meter measurement of an actual component will usually give the necessary information.

Special T-Line, OT-Line and ST-Line Component Entry

The Transmission Line has four "special" versions, in addition to a standard transmission line, for simulation of real devices. The four elements are a microstrip transmission line, a coaxial transmission line, a balanced transmission line and a delay line.

The Open Stub and Shorted Stub have all of these special versions except the Delay Line.

Any of these four elements are defined by first selecting the T-Line device from the standard component menu. Unless the T-Line device is displayed on the menu/prompt line then the "M" key must be pressed first to display it. The first T-Line entry prompt for the line impedance also lists "Special". By pressing "S" the new component prompt line is displayed as shown below:

Microstrip Balanced Stripline Coaxial Line Delay Line

Any of these four special T-Line forms is selected in the normal fashion by pressing the highlighted letter of the name as displayed.

Modeled Components

The variations of actual components made are much greater than could be contained within LCAS. This requires the modeling of components from the elements provided within LCAS.

There are two general types of modeled components. Those which model basic elements, such as tapped inductors, and those that model specific devices, for example an LM318 op-

amp. Both types are built the same way, and are discussed as appropriate in each element type.

Two basic component types covered are mutually coupled and tapped inductors discussed in the transformer element (X-former), and the Operational Transconductance Amplifier (OTA) discussed in the Op-Amp element.

Phase Locked Loop Components

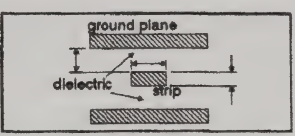
A unique group of components defined in LCAS are the elements of Phase Locked Loop (PLL) circuits. They provide a powerful added capability. These components may not be considered "linear" by themselves, but the complete phase locked loop they represent normally exhibits a linear response vs. frequency. The modeling of these components in LCAS gives analysis capability outside the reach of most other linear analysis tools.

The PLL devices included in LCAS are:

Phase Detector
Loop Amplifier
Voltage Controlled Oscillator
Divide by N

The uses and design of phase locked loops is beyond the scope of this manual. For more information on the design of phase locked loops, consult textbooks available at your local technical library, or from component manufacturers. Appendix D of this manual contains a mini-tutorial on the use of PLL components within LCAS and contains modeling information for typical actual phase locked loop components.

Balanced Stripline -



TYPE	SPECIFICATIONS		COMPONENT NODES			
T-Line	Zo =	1/4W =	-In =	+In =	-Out =	+Out =

External nodes: 4 **Internal nodes: 0**

Description

The Balanced Stripline is a special case of the transmission line, open or shorted stub elements. It is selected by first selecting the appropriate type line (either transmission, open or shorted stub) and then pressing "**S**" for special and "**B**" for balanced stripline.

The balanced stripline consists of a center conductor strip located equidistant between two ground planes. The intervening space consists of a dielectric material.

Entries The Impedance (Zo) and 1/4 wavelength of the line are calculated by LCAS from the following five entries: Negative values are not allowed.

Dielectric Constant The dielectric constant of the material used between the center conductor strip and ground planes.

Dielectric Thickness The distance between the center conductor strip and the ground plane, in inches.

Line Thickness The thickness of the center conductor strip in inches.

Line Width The width of the center conductor strip in inches.

Line Length The length of the center conductor strip in inches.

Nodes The input and output nodal connections. The balanced stripline is bi-directional. The plus and minus indicators are used for phasing. By convention the plus in and out represent the center conductor strip. Balanced stripline stubs do not require entry of the "out" nodes.

Notes

The balanced stripline element is useful in simulating stripline traces used in specially fabricated circuits. The technique of building balanced striplines as part of the circuit structure is common at frequencies of approximately 1 GHz and above.

During entry the limits for each value entry are calculated and presented based on previous entries. You may "back-up" during parameter entry using the **[Esc]** or left arrow key.

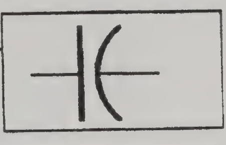
The approximations used to calculate the impedance and 1/4 wavelength of the line from the entered parameters are those presented by Dr. I. J. Bahl and Ramesh Garg as published in "Microwaves", January issue, 1978, starting on page 90.

The characteristics of some common materials and circuit board types are listed below for reference only. You should consult manufacturer's information to determine the specifications of the specific materials being used. At very high frequencies (10 GHz and above) the dielectric constant entry may be modified to correct for known errors due to dispersion.

Board/Material	Dielectric Constant
Fiberglass FR4/G10	4.5 to 5.5
Teflon impregnated glass or Duroid®	2.2 to 2.6
Polycarbonate	3.0
Polyethylene	2.3
Polystyrene	2.6
Aluminum oxide	8.8
Porcelain	5.8

If only the copper weight on a pcb is known, the line thickness may be computed as approximately 0.00135 inches per ounce. i.e. 2 ounce copper has a thickness of 0.00270 inches.

Capacitor -



TYPE	SPECIFICATIONS		COMPONENT NODES			
Cap	Value=	Qp=	Node	Node	▨	▨

External nodes: 2

Internal nodes: 0 if parallel or infinite Q, **1** if series Q is specified.

Description

The Capacitor element provides a capacitive reactance that is either perfect (without loss) or with a prescribed Q, representing a real world lossy capacitor between the two nodes indicated by the user.

Entries

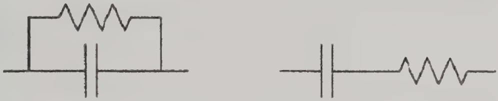
Value= Capacitance in Farads. Use engineering or scientific notation. Negative values may be used to simulate special conditions.

Qp=(or Qs=) Element Q factor. Pressing **[Return]** or the right arrow key defaults to an infinite Q. A direct value entered results in a parallel resistor addition. If the entry is preceded by "S" then the value results in a series resistor addition. In either case LCAS reminds you of the present connection by using "**Qp=**" or "**Qs=**" in the specification cell. See the notes below.

Nodes The order of nodal entry is not critical.

Notes

Q may be modeled as either a parallel or series loss by preceding the Q entry with the letter "P" or "S" respectively. Therefore an entry of "P100" defines a capacitor with a parallel loss and an entry of "S100" defines a capacitor with a series loss, both having a Q of 100. Negative Q values are not allowed. If no letter is specified then parallel loss is assumed. If no value or a value of zero is specified then a Q of infinity is assumed.



Parallel Series

Capacitance "Q" Models

The formulas LCAS uses to calculate the parallel or series resistor are:

$$R = \frac{Q}{2 \pi f_m C} \qquad \text{Parallel resistor}$$

$$R = \frac{1}{2 \pi f_m C Q} \qquad \text{Series resistor}$$

where f_m is the frequency mean or median calculated by:

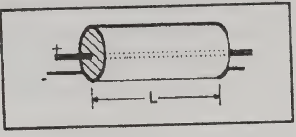
$$f_m = \sqrt{f\,\text{start} \bullet f\,\text{stop}}, \quad \text{Sweep} = \text{Log}$$

or

$$f_m = (f\,\text{start} + f\,\text{stop})/2\,, \quad \text{Sweep} = \text{Linear}$$

The value of f_m does not change when an expanded analysis is performed.

Coaxial Line -



TYPE	SPECIFICATIONS		COMPONENT NODES			
T-Line	Zo=	1/4W=	-In=	+In=	-Out=	+Out=

External nodes: 4 **Internal nodes: 0**

Description

The Coaxial line is a special case of the transmission line, open or shorted stub elements. It is selected by first selecting the appropriate type line (either transmission, open or shorted stub) and then pressing "S" for special and "C" for Coaxial line.

The coaxial line presents a straightforward method of using a specific length of coax when the line impedance and velocity factor are known.

Entries

Zo= Line Impedance in Ohms. This is the characteristic impedance of the coaxial cable. Negative values are allowed.

The following two entries are used by LCAS to calculate the effective 1/4 wavelength of the coax.

Line Length The physical cable length in inches.

Velocity Factor The ratio of the velocity of propagation in the coax to that of light in free space. Values must be between .001 and 1. Typical cables are in the range from 0.5 to 0.95. Negative values are not allowed.

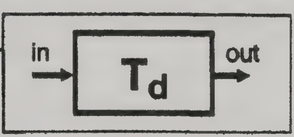
+/- In=(Out=) Nodes The input and output nodal connections. The coaxial line is bi-directional. The plus and minus indicators are used for phasing. By convention the plus in and out represent the center conductor and the minus in and out nodes represent the shield and would typically be connected to node 0. Coaxial stubs do not require entry of the "out" nodes.

Notes

The coaxial transmission line can directly simulate common or imaginary coaxial cables. The characteristic impedance and velocity of propagation for several typical coax cables is given below for reference. The velocity of propagation is mainly a function of the center conductor insulation material, where polyethylene typically yields 0.66 and cellular polyethylene yields 0.78. Consult the cable manufacturer's specifications for your type as specifications often vary by manufacturer.

Cable	Impedance	Velocity Factor
RG-6/U	75Ω	0.78
RG-8/U	52Ω	0.66
RG-8/U	57Ω	0.78
RG-11/U	75Ω	0.66
RG-58/U	50Ω	0.66
RG-58A/U	50Ω	0.78
RG-59/U	73Ω	0.66
RG-59A/U	75Ω	0.78
RG-62/U	93Ω	0.84
RG-174/U	50Ω	0.66
RG-213/U	50Ω	0.66
RG-214/U	50Ω	0.66
1/4" Heliax	50Ω	0.79
1/2" Heliax	50Ω	0.88

Delay Line -



TYPE	SPECIFICATIONS		COMPONENT NODES			
T-Line	Td=	Av=	In=	Out=	▨	▨

External nodes: 2 **Internal nodes: 0**

Description

The Delay Line is a special case of the transmission line element. It is selected by first selecting the transmission line and then pressing "S" for special and "D" for Delay line.

The Delay line is used to introduce a time delay into a circuit at a specific point.

Entries

Td = Time delay in seconds. Negative values are not allowed.

Av= Gain in Volts/Volt. Values can either be positive or negative. Pressing the [Return] or right arrow key defaults to a gain of 1.0.

In=(Out=) Nodes The input and output nodal connections. The delay line is not bi-directional, so node entry order is important.

Notes

The Delay Line has an infinite input impedance and an output impedance of 0.1 Ohm.

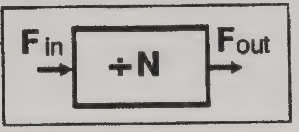
The delay element is useful in making transversal filters and as an element in phase locked loop circuits where the delay can be used to simulate digital circuit delay times or long feedback loops. Also see the divider for PLL delay.

Most digital filter implementations use delay elements with weighted tap coefficients. This technique is easily modeled within LCAS. The only limitation is that in digital filters, numbers must be of finite word lengths. LCAS with an 8087 supports 80 bit word lengths, somewhat better than reasonable hardware implementations. Therefore filters modeled in LCAS perform quite well, but when built with significantly truncated word lengths may be degraded.

Tapped delay lines can be constructed of multiple series connected delay line elements.

See Appendix F for example circuits using the Delay Line. The RD_BW circuit is a 2 pole Butterworth lowpass filter and the FWD_TRAN circuit is a non-recursive, N=10, hanned transversal lowpass filter.

Divide by N -



TYPE	SPECIFICATIONS		COMPONENT NODES			
÷N	N=	Td=	Fin=	Fout=	▨	▨

External nodes: 2

Internal nodes: 0
1 if delay > 0

Description

The divide by N element is used on either or both of the phase detector inputs to scale the reference or VCO frequency. The divider may be used as a multiplier by making the N value less than one. The divider can also introduce time delay into the PLL for simulation of divider delay or "long" loops.

Entries

N= Divide ratio. Divisors do not have to be integer, and may be negative. A value between 0 and 1 results in a multiplie rather than divider.

Td= Time delay in seconds. The time delay defaults to 0.0 seconds if either the **[Return]** or right arrow key is pressed at this entry. The time may be zero but not negative.

Nodes. The input and output nodal connections, labeled frequency in and out.

Notes

The input impedance is infinite and the output impedance is 0.1 Ohm.

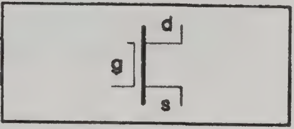
The Divide by N element is non-inverting.

To model a frequency multiplier simply enter the inverse of the multiplier factor. For example to model a times five multiplier, the entry should be 1/5, entered as 0.2.

An example file of a phase locked loop using the divider (named "LOOP") is included on the master diskette.

For more information on the Divide by N use in phase locked loop circuits see Appendix D.

FET -



TYPE	SPECIFICATIONS		COMPONENT NODES			
FET	Gm =		Gate =	Srce =	Drain =	

External nodes: 3 **Internal nodes: 0**

Description

The Field Effect Transistor element provides a generic device capable of simulating any single gate FET, either N or P channel. The FET represents an ideal transconductance.

Entries

Gm = Transconductance in mhos (1/Ohms). Gm is equal to Iout/Vin. Values can either be positive or negative. Negative values provide a non-inverting transconductance.

Nodes Connections for the gate, source and drain. The source and drain are not interchangeable. See notes.

Notes

1mho = 1 Amp/Volt.

Normally the transconductance is inverting through the FET but by use of a negative Gm value it is non-inverting. This can be useful for analyzing a specific node for its impedance or for scaling signal levels on passive circuits with source and terminating impedances (see the Tips and Techniques Appendix).

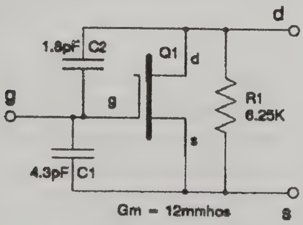
The transconductance is not dependent on any operating conditions as it would be using a real world device, so take care not to over estimate the performance of a particular circuit until you have varied this parameter over the ranges that will actually be encountered.

The gate and drain impedance is infinite. This element is an ideal FET, it is perfectly linear, has no internal feed-back, is insensitive to frequency and is completely independent of external forces.

Caution, typical FETs are symmetrical, allowing the source and drain to be swapped with little effect. This does not hold true here, the gate and drain are always relative to the source for forward transconductance.

To approximate a real world FET it is usually necessary to model the particular device being used. This can be done, generally, by placing resistors and capacitors between the terminals of the ideal FET element to represent the real world terminal impedances. This method is often useful to several tens of megahertz. Once modeled it can be saved and later used again by merging it into your circuit as you are creating it.

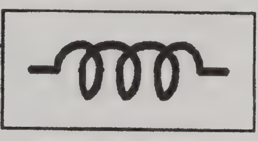
Example - J310 RF FET Modeled @ Id = 10mA



C1 = gate to source capacitance
C2 = gate to drain capacitance
R1 = 1/Gos, or output resistance

Note, this is just one general form, a FET can be modeled in several different ways and to any level of accuracy required.

Inductor -



TYPE	SPECIFICATIONS		COMPONENT NODES			
Induc	Val=	Qs=	Node	Node	▨	▨

External nodes: 2

Internal nodes: 0 if parallel or infinite Q, 1 if series Q specified.

Description

The inductor element provides an inductive reactance that is either perfect (without loss) or with a prescribed Q, representing a real world lossy inductor, between the two nodes indicated by the user.

Entries

Value= Inductance in Henrys. Use engineering or scientific notation. Negative values may be used to simulate special conditions.

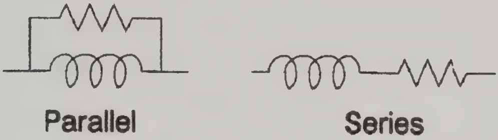
Qs= (or Qp=) Element Q. Pressing **[Return]** or the right arrow key defaults to an infinite Q. A direct value entered results in a series resistor addition. If the entry is preceded by "**P**" then the value results in a parallel resistor addition. In either case LCAS reminds you of the present connection by using "Qp=" or "Qs=" in the specification cell.

Nodes The order of nodal entry is not critical.

Notes

Special types of inductors such as tapped inductors and mutually coupled inductors are simulated using the transformer element. See the "X-former" element in this chapter for more details.

Q may be modeled as either a parallel or series loss by preceding the Q entry with the letter "P" or "S" respectively. Therefore an entry of "P100" defines an inductor with a parallel loss and an entry of "S100" defines an inductor with a series loss, both having a Q of 100. Negative Q values are not allowed. If no letter is specified then series loss is assumed. If no value or a value of zero is specified then a Q of infinity is assumed.



Inductance "Q" Models

The formulas LCAS uses to calculate the series and parallel resistor values to place in these circuit models are:

$$R = 2\pi f_m L Q \qquad \text{Parallel resistor}$$

$$R = \frac{2\pi f_m L}{Q} \qquad \text{Series resistor}$$

where f_m is the frequency mean or median calculated by:

$$f_m = \sqrt{f\,\text{start} \bullet f\,\text{stop}}, \quad \text{Sweep} = \text{Log}$$

or

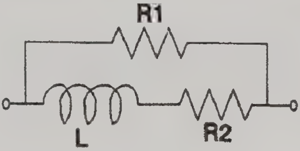
$$f_m = (f\,\text{start} + f\,\text{stop})/2, \quad \text{Sweep} = \text{Linear}$$

The value of f_m does not change when an expanded analysis is performed.

For circuits that require the utmost in accuracy, an inductor can be modeled with both a series and parallel loss. The only requirements are that the peak Q and frequency that the Q peaks at are known. Modeling an inductor by this method requires the addition of two external resistors and the use of the following equations:

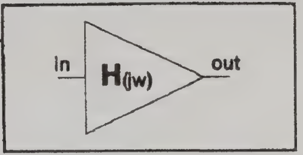
$$R1 = 4 \pi f L Q$$

$$R2 = \frac{\pi f L}{Q}$$



Where, f = frequency at which Q is at its peak
L = Inductance of the inductor being modeled
Q = Peak Q at frequency f

Loop Amplifier -



TYPE	SPECIFICATIONS		COMPONENT NODES			
LoopAmp	BW=	Fz=	In=	Out=		

External nodes: 2 **Internal nodes: 2**

Description

The Loop Amplifier element is intended to be used as a Phase Locked Loop component. It is normally placed between the phase detector output and the VCO control input. The characteristics assigned to the Loop amplifier are a major determinant of the PLL response.

Entries

BW= Unity gain bandwidth in Hertz. This value does not include the effect of the response zero given below. Negative values are not allowed.

Fz= Frequency of the response zero in Hertz. Negative values are not allowed.

Nodal connections For the input and output. Unlike an operational amplifier, the loop amplifier has only a single input and output. It is also non-inverting.

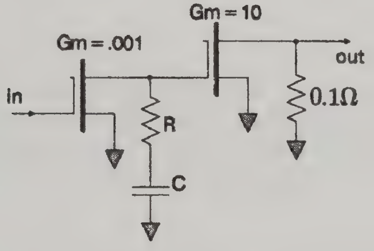
Notes

The loop amplifier has an infinite input impedance and a 0.1 Ohm output impedance.

The loop amplifier is intended for but not restricted to use in phase locked loop circuits as part of second and third order loops. It has a single pole at zero frequency and a single zero at Fz.

The loop amplifier is non-inverting unlike typical op-amp loop amplifiers. Therefore, if this device is substituted for an inverting op-amp in a PLL, then a negative gain in the companion phase detector or swapping the phase detector inputs is required to re-invert the signal, providing negative feed-back.

A model of the internal construction of the loop amplifier is shown in the schematic below.



The values for R and C are calculated by -

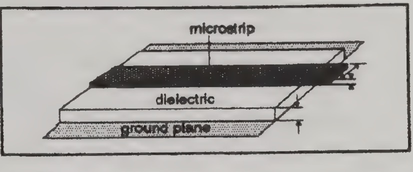
$$C = \frac{1}{2000 \pi Fz}$$

$$R = \frac{1}{2 \pi C BW}$$

The sample file "LOOP" included on the master diskette gives an example of the typical application of the loop amplifier in a phase locked loop. See Appendix F.

For more information on the use of the loop amplifier in phase locked loop circuits refer to Appendix D.

Microstrip Line -



TYPE	SPECIFICATIONS		COMPONENT NODES			
T-Line	Zo=	1/4W=	-In=	+In=	-Out=	+Out=

External nodes: 4 **Internal nodes: 0**

Description

The Microstrip line is a special case of the transmission line, open or shorted stub elements. It is selected by first selecting the appropriate type line (either transmission, open or shorted stub) and then pressing "S" for special and "M" for Micro strip line.

The microstrip line is used to define a form of transmission line typically built onto the structure of printed circuit boards or ceramic materials. It is defined by the geometry of the structure. The microstrip consists of a strip of conductor above a ground plane, separated by a dielectric material.

Entries The Impedance (Zo) and 1/4 wavelength of the line are calculated by LCAS from the following five entries: Negative values are not allowed.

Dielectric Constant The dielectric constant of the material used between the conductor strip and ground plane.

Dielectric Thickness The distance between the conductor strip and the ground plane in inches.

Line Thickness The thickness of the conductor strip in inches.

Line Width The width of the conductor strip in inches.

Line Length The length of the conductor strip in inches.

Nodes The input and output nodal connections. The Microstrip line is bi-directional. The plus and minus indicators are used for phasing. By convention the plus in and out represent the conductor strip. Microstrip stubs do not require entry of the "out" nodes.

Notes

During entry the limits for each value entry are calculated and presented based on previous entries.

You may "back-up" during parameter entry using the **[Esc]** or left arrow key.

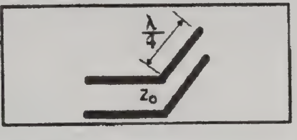
The approximations used to calculate the impedance and 1/4 wavelength of the line from the entered parameters are those presented by Dr. I. J. Bahl and D. K. Trived as published in "Microwaves", May issue, 1977, starting on page 174.

The microstrip transmission line, open and shorted stubs are useful in making circuit board traces as elements of a circuit, or for determining the effect of traces on the operation of a circuit. The characteristics of some common materials and circuit board types are listed below for reference only. You should consult manufacturer's information to determine the specifications of the specific materials being used.

Board/Material	Dielectric Constant
Fiberglass FR4/G10	4.5 to 5.5
Teflon impregnated glass or Duroid®	2.2 to 2.6
Polycarbonate	3.0
Polyethylene	2.3
Polystyrene	2.6
Aluminum oxide	8.8
Porcelain	5.8

If only the copper weight on a pcb is known, the line thickness may be computed as approximately 0.00135 inches per ounce. i.e. 2 ounce copper has a thickness of 0.00270 inches.

OT-Line or Open Stub -



TYPE	SPECIFICATIONS		COMPONENT NODES			
OT-Line	Zo=	1/4W=	-In=	+In=	▨	▨

External nodes: 2 **Internal nodes: 0**

Description

The Open Stub element is a transmission line with a single port. The other end of the line is considered "open".

Special balanced stripline, coaxial and microstrip versions of the open stub are available if parameters for that line type are known.

Entries

Zo= Characteristic impedance in Ohms. Negative values may be used to simulate special conditions.

1/4W= One quarter wavelength frequency in Hz. Negative values are not allowed.

Nodal connections For the + and - inputs. The two inputs are symmetrical but, if one side of the line is grounded, by convention it would be the negative side.

Notes

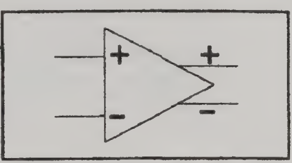
The characteristic impedance of the open stub is equivalent to $\sqrt{L/C}$ where L and C are the inductance and capacitance per unit length.

1/4 Wave or 90° frequency is in Hertz. Negative values are not allowed. This entry provides the effective length of the open stub. The 1/4 wave frequency can be calculated from the length, L, using the formulas:

1/4 wave freq. (MHz) = 2950/L(inches) = 246/L(ft)
(kHz) = 2,950,000/L(inches) = 246,000/L(ft)

If the physical dimensions of a particular type of open stub are known then use the appropriate special versions of open stub available. They are a balanced stripline, coaxial cable and microstrip. See these special versions in this section for more specifics.

Operational Amplifier -



TYPE	SPECIFICATIONS		COMPONENT NODES			
Op-Amp	Av=	BW=	-In=	+In=	-Out=	+Out=

External nodes: 4 **Internal nodes: 0**

Description

The Op-amp element provides a differential input, differential output operational amplifier. Both the open loop DC gain and gain bandwidth product are user defined.

Entries

Av= Open loop gain in Volts/Volt. Negative values may be used to simulate special conditions.

BW= Frequency of the unity gain point in Hertz. An infinite bandwidth may be specified by entering "0". Negative values are not allowed.

Nodal connections for the + and - inputs and outputs. The minus output is the opposite phase of the plus output and is available on some amplifiers. This amplifier has a true differential output having no reference to ground. For a single ended output representation the unused output (normally the -) is connected to ground, node 0.

Notes

Open loop DC gain is in Volts/Volt. Values can either be positive or negative. Typical values for a few common amplifier types are given below.

For general purpose amplifiers a specific gain can be entered in a circuit utilizing no feed-back to provide a fixed gain of that value. See the example configuration below.

Normally the unity gain frequency (the frequency at which the amplifier has no gain or loss) is known, but for amplifiers where only the pole or break frequency is known then use the following equation to determine the proper unity gain frequency (This assumes a single pole, if there are additional poles, they must be modeled externally. Note this might be most easily achieved by cascading multiple Op-Amps, each with its own pole and a combined gain equal to the desired total).

$$BW = A_v \bullet f_p$$

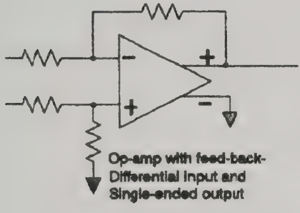
Where, BW = Unity gain bandwidth freq. in Hertz
A_v = Open loop DC gain
f_p = Pole freq. in Hertz

The input impedance and common mode rejection are both infinite. The output impedance, between the plus and minus outputs, is 1/10 Ohm resistive and may have a capacitive component depending on the unity gain frequency chosen, if any.

Op-amp Type	Typical Gain	Typical Unity Gain BW
741	200k	1.0 MHz
TL061	6k	1.0
TL081	300k	4.5
LF351	100k	4.0
LM324	100k	1.0
LM318	200k	15

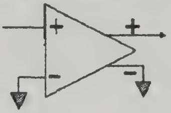
For single ended input operation ground the unused input, for single ended output operation ground the unused output. This makes the appropriate input and/or output relative to ground.

EXAMPLE 1 - The use of the op-amp in a standard configuration with feedback elements, and the use of the op-amp as a gain block element with no feedback are shown below.



Op-amp with feed-back-
Differential Input and
Single-ended output

e.g. for Gain = 15
and 3dB BW = 1MHz
set Av = 15 and BW = 15MHz

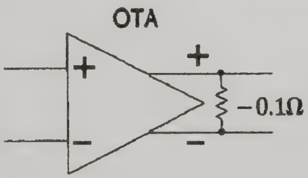


Gain Block
Single-ended Input and output

EXAMPLE 2 - Operational Transconductance Amplifier with single or double ended input and/or output.

The Operational amplifier can also be used to derive an operational transconductance amplifier. The operational amplifier is a voltage amplifier whose output voltage is dependent on the voltage between its two differential inputs. The transconductance amplifier however delivers a current output dependent on the voltage between its two differential inputs.

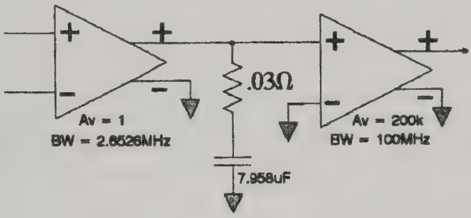
To convert the operational to a transconductance amplifier a resistor is placed between the plus and minus amplifier outputs with a resistance of minus 0.1 Ohm. This cancels the normal op-amps output resistance of 0.1 Ohm.



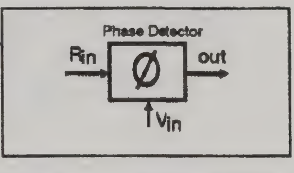
The gain of the Op-amp (Av) now represents 10 times the Gm of the modeled OTA. At the Av prompt therefore, enter 1/10th

of the desired OTA's Gm. The BW entry should be set to infinity.

EXAMPLE 3 - Model of an LM318 Multiple pole op-amp with one zero, differential input and single ended output.


+
−
+
−
Av = 1
BW = 2.6526MHz
.03Ω
7.958uF
+
−
+
−
Av = 200k
BW = 100MHz

Phase Detector -



TYPE	SPECIFICATIONS		COMPONENT NODES			
Ø-det	V/D =	▨	Rin =	Vin =	Out =	▨

External nodes: 3 **Internal nodes: 0**

Description

The Phase Detector element accepts input from two frequencies that are compared in phase, and generates an output which contains magnitude and directional information relative to the two inputs. The two inputs are the Reference and VCO referring to the source of these signals in a PLL circuit.

Entries

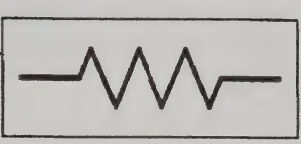
V/D = Detector gain (Kd), or volts of output change per degree of input phase difference. The Kd in volts/radian may be entered by appending "/R" to the value. If already specified in Volts/Radian the input can be set to Volts/Degree by appending "/D". Negative values may be used to simulate special conditions.

Nodal connections. For the reference input (Rin), VCO input (Vin) and output. Swapping the two inputs inverts the output phase.

Notes

The input impedances are infinite and the output impedance is 0.1 Ohm. See Appendix D for typical use in phase locked loops.

Resistor -



TYPE	SPECIFICATIONS		COMPONENT NODES			
Res	Value =		Node	Node		

External nodes: 2 **Internal nodes: 0**

Description

This element provides a purely resistive, non-reactive resistance between the two nodes indicated by the user.

Entries

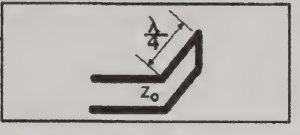
Value= Resistance in Ohms. Use engineering or scientific notation. Negative values may be used to simulate special conditions.

Nodes The order of nodal entry is not critical.

Notes

At high frequencies a capacitor and/or inductor may have to be added to simulate actual resistor characteristics. For instance a wirewound resistor will exhibit both capacitance and inductance.

ST-Line or Shorted Stub -



TYPE	SPECIFICATIONS		COMPONENT NODES			
ST-Line	Zo=	1/4W=	-In=	+In=	▨	▨

External nodes: 2 **Internal nodes: 0**

Description

The Shorted Stub is a transmission line with a single port. The other end of the line is considered "shorted".

Special balanced stripline, coaxial and microstrip versions of the shorted stub are available if parameters for that line type are known.

Entries

Zo= Characteristic impedance in Ohms. Negative values may be used to simulate special conditions.

1/4W= One quarter wavelength frequency in Hz. Negative values are not allowed.

Nodal connections. For the + and - inputs. The two inputs are symmetrical but, if one side of the line is grounded, by convention it would be the negative side.

Notes

The characteristic impedance of the shorted stub is equivalent to $\sqrt{L/C}$ where L and C are the inductance and capacitance per unit length.

1/4 Wave or 90° frequency is in Hertz. Negative values are not allowed. This entry provides the effective length of the shorted stub. The 1/4 wave frequency can be calculated from the length, L, using the formulas:

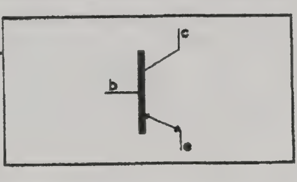
1/4 wave freq. (MHz) = 2950/L(inches) = 246/L(ft)
(kHz) = 2,950,000/L(inches) = 246,000/L(ft)

If the physical dimensions of a particular type of shorted stub are known then use the appropriate special versions of shorted stub available. They are a balanced stripline, coaxial cable and microstrip. See these special versions in this section for more specifics.

High frequency amplifiers can use stub devices for modeling impedance matching networks.

Comb-line filters can be modeled as a series of stub elements with coupling capacitors. See the example circuits on the master diskette labeled "COMB_3" and "COMB_7"

Transistor -



TYPE	SPECIFICATIONS		COMPONENT NODES			
Trans	Beta =	R(b-e) =	Base =	Emit =	Col =	▨

External nodes: 3 **Internal nodes: 0**

Description

The Transistor element provides a first order bipolar transistor. The transistor is a generic element that may be considered either NPN or PNP. Both beta and R(b-e) are user defined.

Entries

Beta = Device Beta and is equal to Ic/Ib or the forward current transfer ratio. Values can either be positive or negative.

R(b-e) = Base-emitter junction resistance in Ohms.

Nodal connections. for the base, emitter and collector.

Notes

Note the Beta is not dependent on any operating conditions as it would be using a real world device, so take care not to over estimate the performance of a particular circuit until you have varied this parameter over the ranges that will actually be encountered.

The R(b-e) resistance is mainly dependent on the junction material, junction temperature and collector current. This information can usually be located in a transistor data book under small signal characteristics. Look for the h parameter h_{ie} or input impedance where common emitter configuration is indicated. For silicon devices this can be approximated by using the following equation:

$$R(b\text{-}e) = (Kt/q) \bullet Beta/Ic$$

Where, R(b-e) = Base-emitter resistance, in Ohms
Beta = Collector current/Base current
Ic = Average collector current, in Amperes
Kt/q = 0.026 at 25°C
Where,
K = Boltzmann's constant, $1.38 \bullet 10^{-23}$
t = Temperature in Kelvin, (298.2°K = 25.0°C)
q = Charge of an electron, $1.602 \bullet 10^{-19}$

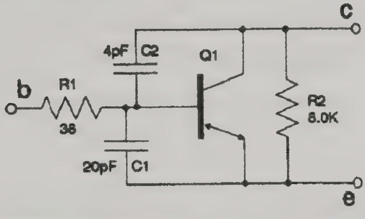
Typical entries for several common transistor types are given below if no other information is available. These values are intended to be used as a guide and should only be used in non-critical analysis.

Generic Type	Beta at mA	R_{b-e}
small signal npn	190 @ 1	5k
	250 @10	700
	100 @ 100	100
medium power npn	170 @ 10	600
	150 @100	200
	80 @500	100
high power npn	80 @ 1000	75
RF amp	70	100

The collector impedance is infinite. This element is an ideal transistor, it is perfectly linear, has no internal feed-back, is insensitive to frequency and is completely independent of external forces. To approximate a real world transistor, especially at

higher frequencies, it is usually necessary to model the particular device being used. This can be done, generally, by placing resistors and capacitors between terminals of the ideal transistor element to represent the real world junction impedances. This method is often useful to several tens of megahertz. Once modeled it can be saved and later used again by merging it into your circuit as you are creating it.

Example - 2N2222A Modeled @ Ic = 10mA



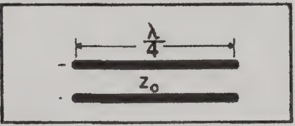
Q1 Beta = 150, R(b-e) = 662 Ohms, Ic = 10 mA

C1 = base-emitter capacitance
C2 = collector-base capacitance
R1 = Cc • Rb/C2
R2 simulates the output impedance
The R(b-e) shown is the actual R(b-e) minus R1

Cc • Rb = collector–base time constant
(Typically ≤ 150pS for a 2N2222A transistor)

Note, this is just one general form, a transistor can be modeled in several different ways and to any level of accuracy required.

Transmission or T-Line-



TYPE	SPECIFICATIONS		COMPONENT NODES			
T-Line	Zo=	1/4W=	-In=	+In=	-Out=	+Out=

External nodes: 4 **Internal nodes: 0**

Description

Purpose: This element provides either a two port bidirectional transmission line that may be characterized in several different ways or a unidirectional delay line with both delay time and gain user defined.

Entries

Zo= Characteristic impedance in Ohms. Negative values may be used to simulate special conditions.

1/4W= One quarter wavelength frequency in Hz. Negative values are not allowed.

Nodal connections. For the + and - inputs and outputs. The two inputs and outputs are symmetrical but, if one side of the line is grounded, by convention it would be the negative side.

Notes

Do not use the Transmission Line to represent an open or shorted transmission line. Instead use the stub devices.

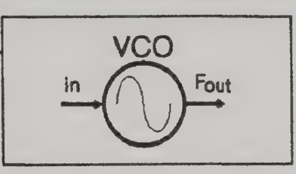
The characteristic impedance of the transmission line is equivalent to $\sqrt{L/C}$ where L and C are the inductance and capacitance per unit length.

1/4 Wave or 90° frequency is in Hertz. Negative values are not allowed. This entry provides the effective length of the transmission line. The 1/4 wave frequency can be calculated from the length, L, using the formulas:

1/4 wave freq. (MHz) = 2950/L(inches) = 246/L(ft)
(kHz) = 2,950,000/L(inches) = 246,000/L(ft)

If the physical dimensions of a particular type of transmission line are known then use the appropriate special versions of transmission line available. They are a balanced stripline, coaxial cable, microstrip. There is also a special delay line version of the transmission line. See these special versions in this section for more specifics.

VCO -



Voltage Controlled Oscillator

TYPE	SPECIFICATIONS		COMPONENT NODES			
VCO	F/V =		In =	Fout =		

External nodes: 2 **Internal nodes: 1**

Description

The VCO produces a frequency that is dependent on the input voltage. As shown in the sample circuits, the VCO normally derives its input control voltage from the Loop amplifier. Specification of the VCO requires:

Entries

F/V = Gain factor in Hertz per Volt, or the frequency change per Volt. Negative values may be used to simulate special conditions.

Nodal connections. Input voltage control nodal connection and output nodal connection.

Notes

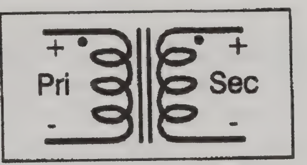
The VCO input impedance is infinite and the output impedance is 0.1 Ohm.

The VCO element is non-inverting.

An example file of a phase locked loop using the VCO is included on the master diskette under the name "LOOP.

Refer to Appendix D for more information on the typical use of VCOs in phase locked loops. The VCO element may also be used as an FM modulator as described in Appendix D under "Loop Tracking".

X-Former (Transformer)-



TYPE	SPECIFICATIONS		COMPONENT NODES			
Xformer	Tp=	Ts=	-Pri=	+Pri=	-Sec=	+Sec=

External nodes: 4 **Internal nodes: 1**

Description

The transformer element is an ideal two port bi-directional device providing impedance matching (voltage and current transforming) determined by its turns ratio. No inductance is represented by the transformer element.

Entries

Tp= Number of primary turns. Negative values invert the phasing.

Ts= Number of secondary turns. If only the turns ratio is known then those numbers may be used directly. No parameters are computed using the specific number of turns in the primary or secondary, but instead are computed from the ratio only. Negative values invert the phasing.

Nodal connections. For the + and - connection of the primary and secondary of the transformer. The + and - designations indicate phasing. The transformer is bi-directional and the terms primary and secondary are for convenience only.

Notes

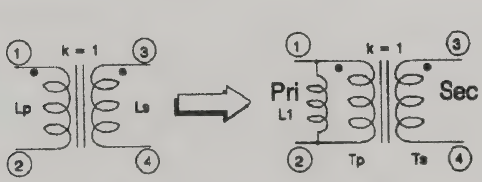
The absolute value of the number of primary and secondary turns is not important, only the ratio between them determines the characteristics of the transformer. The number of turns can either be positive or negative. Entering a negative number of primary turns for example, indicates the turns are rotating opposite a positive value and simply results in effectively swapping the + and - primary node connections.

The primary to secondary isolation and internal impedances are infinite. This element is an ideal transformer, it is perfectly linear, has no inductance, a coupling coefficient of 1 and is insensitive to frequency. By adding additional components it can be made to represent a real world transformer, mutually coupled inductors with a prescribed coupling coefficient or a tapped inductor. These configurations can be determined by using the following examples:

Transformer Models

Transformers with Inductance

Transformers with inductance are generated by placing an inductor in parallel with the primary of a transformer. The real device on the left of the following figure is modeled using a transformer and one inductor as shown, and the following equations:

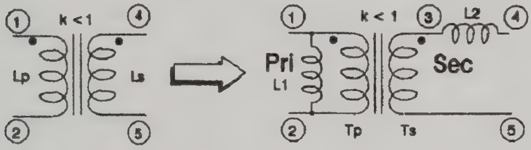


L1 = Lp with the secondary open

$Ls = L1 \bullet (Ts/Tp)^2$

Mutually Coupled Inductors

To simulate mutually coupled inductors where the coupling coefficient is less than 1 the turns ratio of the transformer is modified and an inductor is added in series with the secondary of the transformer as shown below



The formulas for computing the turns ratio and inductances are:

$$Tp = \frac{\sqrt{Lp/Ls}}{k}$$

$$L1 = Lp$$

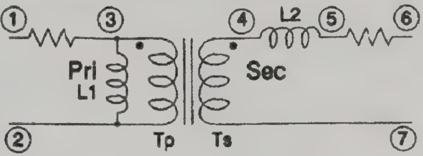
$$L2 = Ls-(Lp/Tp^2)$$

Where, $Ts = 1.0$
Lp = Primary inductance with secondary open
Ls = Secondary inductance with primary open
k = Coupling coefficient between inductors

The file XFMR_BP is an example of mutually coupled inductors with a $k = 0.01$

Mutually Coupled Inductors with Loss

When modeling inductors with finite Q, care must be taken to place the loss elements in the proper place. For parallel losses use the inductor's built in Q on both L1 and L2. For series losses use external resistors in series with the primary and secondary of the transformer model representing the winding's wire resistance.

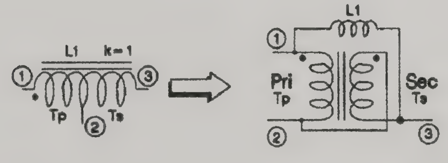


Example of Series Loss Modeling

Tapped Inductors

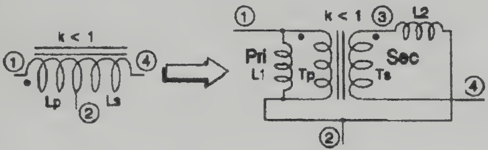
A tapped inductor is simulated by tying one of the primary connections to the secondary. Normally the connection is made from the plus lead of one side of the transformer to the minus on the other side to indicate a continuous winding and phasing. Since the transformer device exhibits no inductance by itself, an inductor must be added separately as shown.

In the case where the coupling coefficient k is equal to 1, the primary and secondary turns of the transformer are the same as that in each side of the tapped inductor. The turns ratio defines the position of the tap. For instance a 1:1 ratio simply means that the inductor is center tapped. The total inductance from the inductors + to - lead is modeled as a single inductor bridging the transformer as shown in the schematic below.



The circuit file DELAY is an example of a tapped inductor with coupling coefficient k = 1

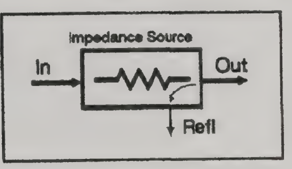
For a tapped inductor with a coupling factor less than 1 the form of model shown below is used.



The computation of the turns ratio and inductor values to simulate a coupling coefficient less than 1 is the same as that used for the mutually coupled inductors with $k < 1$.

The transformer can be used as a return loss measuring device. See Appendix E on "Tips and Techniques" for an explanation.

Impedance Source



TYPE	SPECIFICATIONS		COMPONENT NODES			
Xformer	Zo=	▨	In=	Refl=	Out=	▨

External nodes: 3 **Internal nodes: 0**

Description

The impedance source is a special version of the transformer element providing a user defined output impedance unrelated to the input inpedance. A reflected signal output is also provided that can be used to indicate the return loss, due to mismatch, of a circuit connected to this element's output node. The function is similar to that of a loss-less hybrid.

Entries

Zo= Source impedance (Zout) in Ohms. Negative values may be used to simulate special conditions.

In= The input node, normally specified as the LCAS input.

Refl= The node containing the reflected information. This node may be connected to ground if not being used as the output.

Out= The output node. Normally connected to the circuit to be fed with the specified impedance.

Notes

The impedance source has an infinite input impedance, thus the output impedance is determined strictly by the specified Zo. The reflected signal node has a 0.1 Ohm output impedance.

The reflected signal is relative to the input signal. If the input is not at a 1 VRMS point, such as the LCAS source, then the return loss read at the reflected port will not read directly in dB, but in dB relative to the input.

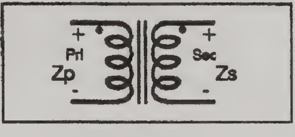
If the reflected signal is not used it should be connected to ground (node 0). Although an error is not produced by leaving it unconnected, this will use one additional node and slow the analysis slightly.

The impedance source was specifically included to allow feeding a circuit with a specified source impedance, while eliminating the 6 dB loss normally associated with using a resistor as the source impedance element. It requires the same number of nodes as a resistor and can be used to replace a resistor source in any existing circuit file.

When analyzing circuits with unequal source and terminating impedances, it is recommended that the circuit under test be terminated with the Matching Transformer element and a load resistor equal to that of the source impedance. The Matching Transformer is used to return the impedance of the circuit's output to that of the source. This allows direct measurement of the circuits power gain or loss.

LCAS analyzes circuits in terms of voltage not power, therefore to measure relative power, the impedances where LCAS is driving and recovering data must be the same. If these impedances are not the same the voltage information provided by LCAS will have to be converted manually into the equivalent power at both the source and termination to determine the circuit's power transfer function. $P = V^2/Z$

Matching Transformer



TYPE	SPECIFICATIONS		COMPONENT NODES			
Xformer	Zp=	Zs=	-Pri=	+Pri=	-Sec=	+Sec=

External nodes: 4 **Internal nodes: 1**

Description

The matching transformer is a special version of the transformer element which performs impedance matching as determined by direct primary and secondary impedance value inputs.

Entries

Zp= Primary impedance in Ohms. Negative values are not allowed.

Zs= Secondary impedance in Ohms. Necative values are not allowed.

Nodal connections. For the + and - connection of the primary and secondary of the transformer. The + and - designations indicate phasing. The transformer is bi-directional and the terms primary and secondary are for convenience only.

Notes

The primary to secondary isolation and internal impedances of this element are infinite. The matching transformer represents and ideal transformer, perfectly linear, insensitive to frequency, with no inductance and a coupling coefficient of 1.

The Matching Transformer element is identical to the Transformer element with the single exception that the number of primary and secondary turns are calculated by LCAS based on the primary and secondary impedance specified. The formulas LCAS uses to calculate the primary and secondary turns are:

$$Ts = \sqrt{Zs/Zp}$$

where, $Tp = 1$
Zp = Primary Impedance in Ohms
Zs = Secondary Impedance in Ohms

One main purpose of the matching transformer is analysis of circuits with unequal source and terminating impedances. It is recommended that the circuit under test be terminated with the Matching Transformer element and a load resistor equal to that of the source impedance. The Matching Transformer is used to return the impedance of the circuit's output to that of the source. This allows direct measurement of the circuits power gain or loss.

LCAS analyzes circuits in terms of voltage not power, therefore to measure relative power, the impedances where LCAS is driving and recovering data must be the same. If these impedances are not the same the voltage information provided by LCAS will have to be converted manually into the equivalent power at both the source and termination to determine the circuit's power transfer function. $P = V^2/Z$

PART 4 -

COMMAND / MENU SUMMARY

Command / Menu Summary

/Analyze

Analyze........ Analyze circuit from Start frequency to End frequency.

Expanded Analysis .... Analyze circuit from lowest graphic marker freq to highest graph marker freq.

/Graph

View Graph Starts the graphing process. Present only in the manual scale mode and before the initial graph. Cannot be "Escaped" from.

New Graph . Erases present graph and generates new scales.
  Add (Last + Present). Adds present data to last graphed data.
  Subtract (Last-Present) ......Subtracts present data from last graphed data.
  Present Only............... Uses present data only.

Overlay Graph .... Retains present graph and scaling factors.
  Add (Last + Present). Adds present data to last graphed data.
  Subtract (Last-Present) ......Subtracts present data from last graphed data.
  Present Only............... Uses present data only.

Graph Data File............ .Graphs analysis results saved previously using /Print Data File Analysis or Graph
  Directory.. Directory of default drive ".DAT" files
  Load......... Loads data file chosen from directory or named. After loading LCAS will return to the /Graph menu

/Graph (Continued)

Set Scale Mode	Allows toggling of following modes.
Automatic	The verrical scales for magnitude and phase/delay are chosen by LCAS to see all data.
Manual	You are allowed to chose the maximum and minimum scale settings for the magnitude and/or phase or delay vertical axis.

/Copy	Copies highlighted components to end of component list and renumbers the copied component nodes. Node 0 remains uneffected.
/Renumber	Renumbers highlighted component nodes by adding a user supplied number. Node 0 remains uneffected.
/Delete	Deletes highlighted components from component list

/Print

Printer	Directs print data to printer port for output.
Analysis Results	The analysis results are output (.PRA)
Components	The component list is output (.PRC)
Graph	The Graph is output (.PRG)

/Print (Continued)

Text File...... Directs print data to default drive for output. File will have the extension ".PRA", ".PRC" or ".PRG".
  Analysis Results .... The analysis results are output (.PRA)

  Components .... The component list is output (.PRC)

  Graph .... The Graph is output (.PRG)

Data File ..... Directs Analysis or Graph numerical results to a file.
  Analysis Results .... The analysis results are output (.PRA)

  Graph .... The Graph is output (.PRG)

FFT File ...... Creates a Fast Fourier Transform file of analysis or graph numerical results.
  Analysis Results .... The analysis results are output in special FFT format. (.F)

  Graph .... The Graph data from the "last" buffer is output in special FFT format (.F)

/Files

Directory..... Provides circuit directory of default drive. All files with the extension of ".LCA" are shown.

Save .... Saves current component list and circuit criteria to default drive. File will have the extension ".LCA".

Load .... Loads component list and circuit criteria from the default drive. Any file with the extension of ".LCA".

Merge.......... Merges component list from the default drive. Any file with the extension of ".LCA".

/Files (Continued)

Erase	Erases circuit file from the default drive. Any file with the extension of ".LCA". The wildcard character "?" may be used with Erase only.
Name	Used to name the circuit file presently in memory. The name then appears on the printer and graphic output, even if the file has not been saved. Saving a file also requests the file name.
Clear	Clears current component list from memory.

/Setup

Co-Processor	Indicates if the 8087 math co-processor installed.
Default Drive	Indicates which disk drive and path is to be used for disk data.
Circuit Files	Specifies the drive/path for circuit files.
Text Files	Specifies the drive/path for text files.
Data Files	Specifies the drive/path for data files.
FFT Files	Specifies the drive/path for FFT files.
Printer	Used to setup the printer port and for special printer modes via setup strings.
Set-Up String	Allows entry of a string of characters to be sent to the printer before each print operation.
Printer Port	Specifies which parallel port a printer is connected to. Either 1, 2 or 3 for LPT1: - LPT3:
Update	Updates configuration file to retain settings.
Exit	Returns to command mode.

/Quit	Exits the LCAS program and return to the operating system.

SPECIAL PURPOSE KEYS

Function Keys

F1	Display component list screen.
F2	Display analysis results (if available).
F3	Display graph (if available).
F4	Prints active screen (formats and prints complete list or graphic).
F5	Starts the analysis of the defined circuit. Equivalent to /Analyze Analyze.
F6	Makes a new graph of the current analysis results. Equivalent to /Graph New Graph Present Only.
F7	Saves the current circuit definition. Equivalent to /Files Save.
F8	Equivalent to /Files Load.
F9	Performs a directory of circuit files on the default drive/path. Equivalent to /Files Directory.
F10	Master escape, Aborts entry at any level. The space bar has same effect in most menus

Control Keys

Esc	Moves back one menu selection level.
Ins	Toggles component insertion mode, allows insertion of component anywhere in component list. Indicated by small "i" on far right of component type menu.
Ctrl	When used with cursor Left/Right keys, on component and analysis result screens it moves cursor extreme left or right, on graphic screen it moves active cursor in coarse steps.

Graph Control Keys

D........................Turns on group delay mode when graph screen is active.

P........................Turns on phase mode when graph screen is active.

N........................Provides noise power information when graph the graph screen is active.

A........................Provides noise power information between markers when the graph screen is active.

J........................Provides phase jitter calculation from a prior noise power calculation using "A" or "N".

Graph Marker Control Keys

1........................Selects Marker one when graph screen is active.

2........................Selects Marker two when graph screen is active.

Up Arrow Key.........Maxima search on active cursor when graph screen is active.

Down Arrow Key....Minima search on active cursor when graph screen is active.

Component Value Edit Keys

x% ....Modifies component values by x percent.

Rx%..................Reverse modifies component by x percent.

PART 5 -

APPENDICES

Appendices Contents

A. Quick Start for Experienced Users
B. Often Overlooked Features
C. Default Settings
D. Modeling Phase Locked Loops
E. Tips and Techniques
F. Example Files
G. Disk File Contents
H. Installation Notes
I. Error Messages
J. Problem Locator
K. Glossary
X. User Support Plan

APPENDIX A

QUICK START FOR EXPERIENCED USERS

Some of you are veteran computer users, already familiar with your computer, DOS, spreadsheets and word processors. If this is the case then you are probably anxious to begin using LCAS immediately, and the detailed instructions are a little too detailed. This Appendix is not intended to be taken as a replacement for reading the manual but should get you started using LCAS very quickly. Well here goes the fast track-

1. LCAS is not copy protected. Make a backup of the master for safekeeping and create a work-disk for everyday use by transferring the file LCAS.EXE to a DOS formatted disk with at least 250K of free space. Alternately place it on your hard disk. We recommend a sub-directory on a hard disk named "DATUM" for the program.

2. Start LCAS from your working copy with the command "LCAS". Within the program you quit using the command "/QY".

3. The command structure of LCAS is similar to spreadsheets. The prompts line is second from the top. Commands begin with the slash key "/", with common commands having function keys assigned. The bottom two lines of the screen are function key reminders. The escape key [Esc] is used to back up from any menu.

4. Configure LCAS using the slash command "/S" for Set-up. Call each of the prompted items in turn to tell LCAS if you have a Numeric Co-processor (8087), the default drive and path for circuit, text, data and FFT files and the printer port and any printer initialization string required. The Update option in this

menu will create a new configuration file (LCAS.INT) on the default drive which LCAS uses to set these items on startup.

5. Draw a schematic for the circuit you wish to analyze. Consecutively number the nodes of the circuit to be analyzed beginning with 1 at the input. Node 0 is the ground or common.

As an example of circuits and node numbering look at the BP circuit in "Part 1, Example Session One". You can load the BP circuit file from the master diskette as a sample using the command "**/FLBP**" representing Files, Load, BP.

6. Components are defined in the component screen by selecting the highlighted letter in the prompt line representing the component desired. Additional components are seen by the "**M**" key. The prompt line prompts for other parameters and nodal connections required. The cursor keys are used to manuever around the screen.

7. Specify the input and output node, the start and stop frequency, and whether a linear or logarithmic increment is desired.

8. Save the circuit created using the slash command **/FS**, using an 8 character or less file name without an extention.

9. Press the **[F5]** function key to perform the analysis. the screen will switch to display the results. When analysis is completed you can scroll thru the analysis using the cursor keys. The **[F1]** function key returns to the component screen, and **[F2]** returns to the analysis results.

10. Press the **[F6]** function key and the analysis results will be graphed. The left and right arrow keys control two graphic line cursors, with corresponding info on the bottom of the graphic screen. To access the second line marker press "2"; pressing "1" will return control to the first line marker.

Pressing "D" when a graph is displayed will change the phase response to a group delay response. Pressing "N" will calculate and display the noise power under the curve relative to the level of the 1st marker. Pressing "A" will calculate the power repre-

sented by the integral of the magnitude response between the two graphic line markers.

[F1], [F2] and [F3] can be used to switch between all three screens.

Reference information on all the components supported directly by LCAS is contained in Part 2.

The Command Summary immediately precedes the Appendicies.

Again, this has only been a very quick discourse on getting started with the LCAS program. There are numerous features not covered here which require that you read the manual to learn about.

The circuit files on the disk can be used for samples and are briefly covered in Appendix F. Appendix B has a list of features in LCAS often overlooked, especially by those who never get around to reading the rest of the manual.

APPENDIX B

OFTEN OVERLOOKED FEATURES

Experience with initial users of the LCAS program showed that there were particular features which seemed to be overlooked most often. The presently known features are listed here simply for reference. The hope is that those persistant souls who absolutly refuse to read a manual will at least glance here and pick up a few tidbits to make life easier.

1. **File Selection.** You don't have to type in file names to load a file. Once a file is saved on disk, first request a directory then press "L" for Load and the first file in the directory list will be highlighted. Use the cursor keys to highlight the correct file and press **[Return]** to load the file. This procedure works with merging circuit files also, and when loading an analysis data file for graphing.

2. **Changing Input/Output Node.** You can change the input and output nodes to see what the response is like at a different point in the circuit. This is just like using an oscilloscope to view different points in a circuit.

3. **Component Menus.** When the component menu/prompt is displayed, using the "M" key will show another set of components. Since some of these components share the same highlighted letter used to invoke the component, you must have the correct menu displayed to select those components.

4. **Noise Power.** When a graph is displayed the noise power represented by the area under the magnitude response can be computed by pressing the "N" key. If marker 1 is placed on the graph an additional computation of the

noise power with reference to marker 1 is accomplished and displayed. See Part 2 for more information.

5. **Area Under the Curve.** The integral of the power represented by the area under the magnitude response curve between two point can be calculated when a graph is displayed. Select the bounds for the freqency limits with the two markers, and press the "A" key. The bottom line of the screen will show the computed power for an input power density of 1 Watt per Hertz. Refer to Part 2 for reference information.

6. **Group Delay.** Normal graphs are drawn with two functions displayed by default, the magnitude and phase responses vs. frequency. To display the magnitude and group delay responses press the "D" key after the initial graph is displayed. To return to the original magnitude and phase response press the "P" key.

7. **Expanded Analysis.** For more detail of a particular area of the graph response, an expanded analysis can be performed. This is the equivalent of zooming in on one area of the graph. After an initial analysis and graph is accomplished, the frequency range to be expanded is bounded using the two graphic markers in the graphic screen. An expanded analysis is then requested by the command "/AE". Refer to the Index for pages with more information.

8. **Graphic Markers.** There are two graphic markers available. the first will move onto the graphic screen if either the right or left arrow keys are pressed. A second marker will become available if the "2" key is pressed and the arrow keys used to position it. Pressing "1" will return control to the first marker. Refer to Part 1 for more information.

9. **Updating the Startup File.** The LCAS startup file, "LCAS.INT", contains that configuration set in the "Set-Up" command. To re-write this file with the current configuration be sure to use the "Update" option from the set-up menu before quitting LCAS.

10. **% Key Operation** The "%" key operator will compute both plus and minus percentage changes in component values and undo those changes simply. An example is given in "Example Session One" of Part 1, and the command described under "Circuit and Component Modification" in Part 2.

11. **Special Purpose Keys.** There is a list of all the special purpose keys in the Command / Menu Summary in Part 4. You may find some overlooked capabilities there.

12. **Insert Key.** A new component can be inserted into the existing list of components, instead of the default overwriting, by using the "insert" key. The insert mode is toggled each time the [Ins] key is pressed. When "ON" a lower case "i" appears at the end of the menu/prompt line when entering components. The cursor is placed at the position where a component is to be inserted and when a new component type is selected those components below the cursor position are pushed down.

13. **Special Test Tools.** Special measurements can be easily accomplished in a circuit using "test tools". Several of these tools are desciribed in Appendix E.

14. **Copying and Renumbering Components.** The definition or modification of certain circuit types can be simplified by using the Copy and Renumber functions provided in LCAS. These two commands are described in the Command Reference, Part 2. An example of renumbering is also given in "Example Work Session Two" in Part 1.

APPENDIX C

DEFAULT SETTINGS

Startup File Defaults

LCAS has certain default setting which are used if no copy of the LCAS.INT file is found in the drive and path from which LCAS was started. These settings are designed to allow operation in any normal hardware configuration. They are:

Default Drive and Path
    Circuit Files - Current drive/path when LCAS is entered.
    Text Files - Current drive/path when LCAS is entered.
    Data Files - Current drive/path when LCAS is entered.
    FFT Files - Current drive/path when LCAS is entered.

Co-processor option - NONE

Printer port - LPT1:

Printer Set-up string - NONE

Monitor type - Automatically selected. Looks for a monochrome adaptor for text and Color/Graphics adaptor for graphics output.

Initial Program Settings

When starting an initial circuit definition from a clear screen after startup, LCAS assumes the following defaults:

Input Node = 1
Number of Data Points = 20
Sweep Mode = LOG
Graph Scale Mode = Auto
Graph Secondary Response = Phase

Subsequent new circuit definitions from a clear screen reset the input node, number of data points and sweep mode as above, but retain the graph scale mode and secondary response from the previous settings.

APPENDIX D

MODELING PHASE LOCKED LOOPS

LCAS is equipped with the ability to analyze phase locked loop circuits. The design of phase locked loop circuits is beyond the scope of this manual, but several examples, tips and techniques are given here to make the use of phase locked loops within LCAS easy.

The phase locked loop (PLL) elements in LCAS provide a quick and simple way to analyze the closed loop characteristics of a PLL. This allows determination of stability, bandwidth and noise performance under varying operating conditions.

The information in this Appendix is separated into three areas:

- Loop Basics
- Modeling Specific Components
- Loop Testing

Loop Basics

Below is an example of a typical PLL showing the connections between elements.

All the PLL elements provided are non-inverting and operate properly if connected directly together. The LCAS program will not analyze certain open loop functions such as acquisition time or frequency step functions since these are non-linear functions.

The PLL shown in Figure D-1 is a 2nd order loop, with a loop natural frequency, fn = 100Hz and a damping factor, ζ = 0.70711. The circuit file for this loop is provided on the master diskette under the name "LOOP".

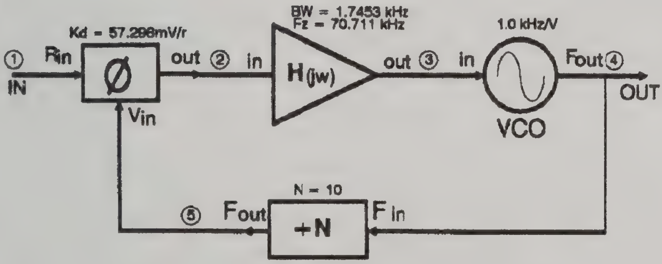

Kd = 57.296mV/r
①
Rin
IN
Ø
Vin
out ②
in
BW = 1.7453 kHz
Fz = 70.711 kHz
H(jw)
out ③
in
1.0 kHz/V
VCO
Fout ④
OUT
N = 10
⑤
Fout
÷N
F in

Figure D-1   Typical Direct Loop Connection

The 2nd order PLL design equations used for this circuit are:

$$BW = \frac{N\,fn^2}{Kd \cdot F/V}$$

and

$$Fz = \frac{fn}{2\,\zeta}$$

Where, Kd = phase detector gain in Volts/radian
F/V = VCO gain in Hertz/Volt
fn = loop natural frequency in Hertz
ζ = damping factor, and
N = divisor

LCAS' input node or excitation point when used in conjunction with the PLL elements represents a carrier that is phase modulated with a one radian RMS sinusoidal signal. The output node or the monitor point acts as a phase demodulator and reads directly in radians RMS of modulation. LCAS' outputs however are given in Volts. Therefore, if at a specific frequency of analysis the output node of a PLL circuit measures a value of 1.2mV it would correspond to a phase deviation of 1.2 milliradians RMS. The frequency of phase modulation is the frequency range choosen for analysis.

The carrier frequency used within LCAS is infinite and therefore does not effect the closed loop characteristics. For real world PLLs the carrier frequency is finite and usually causes both a sampling effect and spurious signals at the output of the phase detector. This sampling effect in addition to spurious signals usually limits the usable loop bandwidth to something significantly less then the sampling frequency (phase detector operating frequency). Therefore, for accurate analysis, the closed loop PLL response should be significantly attenuated at the phase detector operating frequency.

Inside the Loop

In the PLL those nodes between the phase detector output and the VCO input are normally characterized by their voltage, not their frequency components. If LCAS's input node is used to drive nodes between the phase detector output and VCO input it retains its normal characteristic as a one Volt RMS voltage source. Likewise if the output node is used to monitor some point within the same region, it reads in Volts RMS.

This can be very useful to force a known spurious signal level into the loop amplifier and in turn see how much phase modulation there is at the VCO output in terms of either phase deviation in radians RMS or total sideband energy in dBc. The LCAS analysis results listing for magnitude in "Volts" at this point represents phase deviation in radians RMS, and the magnitude in "dB" represents the total sideband energy in dBc (db relative to the carrier). Total sideband energy means that it includes sidebands on both sides of the carrier at the specified frequency. The indication of total sideband energy in dBc should be limited in use to values of -20 dBc or less due to accuracy limitations in the relationship between phase deviation and sideband energy. Signals with a large phase deviation begin to resemble FM type modulation and therefore do not have a direct linear relationship with the total sideband energy.

The loop amplifier element may be substituted for your own loop amplifier design but care must be taken to maintain the proper phasing through out the loop. For example if your loop amplifier design is a typical single op-amp integrator it is probably inverting in nature and will require an aditional inversion somewhere in the loop to provide the required negative feed-back. This can be acomplished by several methods though generally the simplest is to either enter a negative phase detector gain or reverse the Ref and VCO inputs to the phase detector.

All the parasitic poles and zeros normally incountered in the loop being modeled may be placed anywhere between the phase

detector output and the VCO input, representing actual operating conditions. Typical examples of parasitic poles, are resistor coupled varactor diodes in a VCO, a RC lowpass following the phase detector, notch filters to reduce spurious responses and stray capacitances in high gain, high frequency loop amplifiers.

Open Loop Testing for PLL Stability

To check the stability of a particular PLL design, it is usually best to open the loop and observe the gain margin. This can be easly achieved by grounding the phase detector input normally driven from either the divide-by-N or VCO, then connecting LCAS' output node to the node number that was previously connected to the phase detector and re-analyzing the circuit.

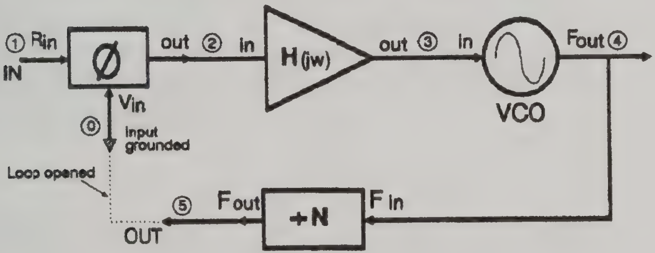


Figure D-2
Typical Open Loop Test Configuration

Locate the frequency (if any) that the open loop phase shift passes through 180 degrees and observe the gain at that frequency. If the gain is greater than or equal to one, it will likely oscillate, if the gain is less than one then it will be unconditionally stable. The gain margin is the difference between the actual circuit gain where the phase passes through 180 degrees and unity gain.

As the gain approaches unity the closed loop response will peak more and more until it becomes unstable. Note that linear cir-

cuit analysis will not necessarily indicate if a particular design will oscillate under closed loop type analysis.

The analysis will peak at infinity only as both the gain passes through unity and the phase passes through 180 degrees. As the gain becomes either greater than or less than unity the peaking will reduce and will appear to be stable even though it may well not be. And as we all know the open loop gain must be less than one to be considered stable at the frequency the phase passes through positive feed-back. This simply means that to determine if a closed loop circuit is potentially unstable, the feed-back loop should be opened and then re-analyzed. If the gain is greater than one as the phase shift passes through 180 degrees it is very likely to be unstable. Note the critical phase shift in these examples is 180 degrees because the two signals feeding the phase detector are supposed to be in phase, if they are 180 degrees out of phase it is positive feed-back and potentially unstable. If the loop is opened and driven directly within the feed-back path the critical phase shift is either 0 or 360 degrees. An exception to this rule is the third order PLL, even though the gain is greater than one and the phase is equal to or greater than 180 degrees, it may well be perfectly stable.

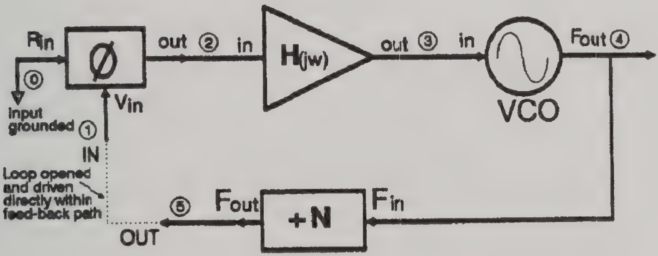


Figure D-3
Opening the Loop and Driving within the Feed-Back Path

Delay in the Loop

The Divide-by-N element allows time delay to be easly modeled within LCAS. Delays may be introduced within the loop due to long divider chains, propagation delays in loops closed around multiple radio tranceivers or in mechanical devices. The time delay is one of the entry parameters of the divide-by-N. Although delay may also be introduced via the delay line special case of the transmission line, the delay provided by the divide-by-N element is normally used in PLL circuits.

Modeling PLL Components

Modeling Phase Detectors

Several types of phase detectors are in common use for PLL circuits. The examples below show methods of modeling the various phase detectors and loop amplifiers.

Linear Multiplier Phase Detector

First is an example of modeling a linear multiplier type phase detector. If the multiplier's gain is not available it can be empirically determined by setting F1 not equal to F2 , and measuring the peak-to-peak voltage of the "beat frequency" at the multiplier output. Do not include the sum frequency of F1 + F2, only the difference or |F1-F2|.

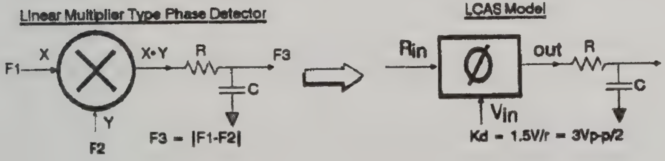

Linear Multiplier Type Phase Detector
F1
X
X•Y
R
F3
C
Y
F2
F3 = |F1-F2|
LCAS Model
Rin
Ø
out
R
C
Vin
Kd = 1.5V/r = 3Vp-p/2

Figure D-4   Linear Multiplier Phase Detector Model

CMOS Exclusive OR Phase Detector

Second is an example modeling a CMOS exclusive OR gate used as a phase detector. Assuming the output load is light, full power supply swing is available at the output. For a 5V power supply the Kd for this type detector is:

$$Kd = \frac{V_{OH} - V_{OL}}{\pi} = \frac{5.0V - 0.0V}{\pi} = 1.5915\ V/r$$

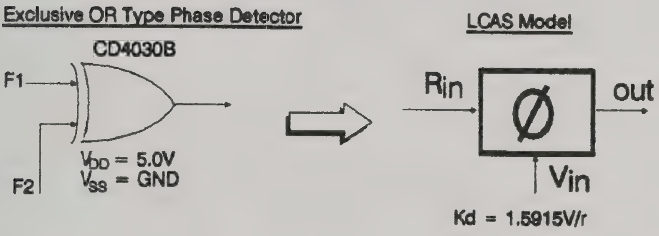
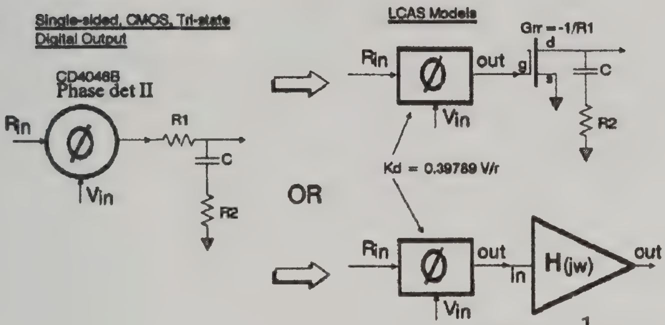


Figure D-5 Exclusive OR Gate Phase Detector Model

CMOS Single Output Phase Detector

Next is one of the standard integrated circuit phase detectors with a single CMOS TRI-state digital output. The second or "II" phase detector in the CD4046 package is modeled in Figure D-5 via two methods. First is the use of a non-inverting FET and RC circuit, and second is the loop amplifier element with parameters. In either case the detector gain is dependant on the supply voltage and is given by:

$$Kd = \frac{V_{DD} - V_{SS}}{4\pi} = \frac{5.0V - 0.0V}{4\pi} = 0.39789\ V/r$$


Single-sided, CMOS, Tri-state Digital Output
CD4046B
Phase det II
Rin
Ø
Vin
R1
C
R2
OR
LCAS Models
Rin
Ø
out
Vin
Gm = -1/R1
d
g
s
C
R2
Kd = 0.39789 V/r
Rin
Ø
out
Vin
in
H(jw)
out

$$BW = \frac{1}{2\pi R1\,C}$$

$$Fz = \frac{1}{2\pi R2\,C}$$

Figure D-6
CD4046B Phase Detector II Single-sided CMOS Output

TTL Dual Output Phase Detector

The MC4044 type phase detector has a dual TTL digital output and typically uses the differential inputs of an op-amp with filtering as its loop amplifier as shown in figure D-7.

Two models are shown for simulation of this type phase detector and loop amplifier combination in LCAS. Both should work the same except note that the phase detector Kd should be negative if an op-amp type loop amplifier is used as in model type A in figure D-8.

The detector gain for either of these models is computed by similar formulas as before:

$$Kd = \frac{V_{OH} - V_{OL}}{2\pi} = \frac{5.0V - 0.4V}{2\pi} = 0.73211 \text{ V/r}$$

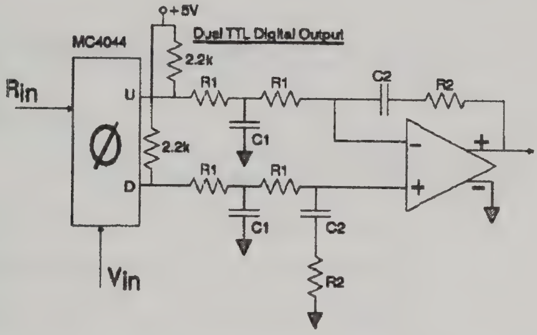
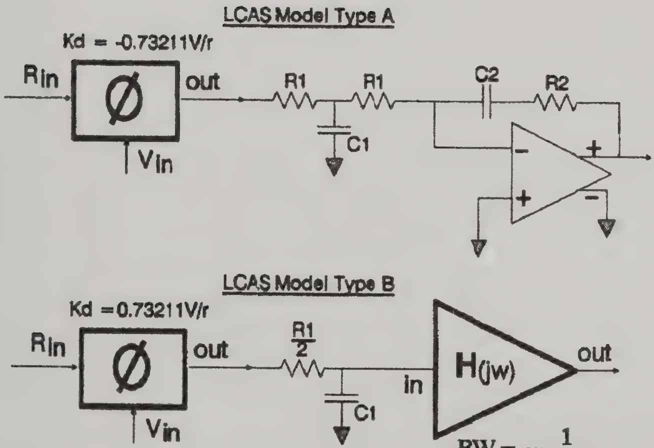

+5V
Dual TTL Digital Output
MC4044
2.2k
Rin
U
R1
R1
C2
R2
Ø
2.2k
C1
D
R1
R1
C1
C2
Vin
R2

Figure D-7
MC4044 Phase Detector with Loop Amplifer


LCAS Model Type A
Kd = -0.73211V/r
Rin
Ø
out
R1
R1
C2
R2
C1
Vin
LCAS Model Type B
Kd =0.73211V/r
Rin
Ø
out
R1/2
in
H(jw)
out
C1
Vin

$$BW = \frac{1}{4\pi R1\,C2}$$

$$Fz = \frac{1}{2\pi R2\,C2}$$

Figure D-8 MC4044 Dual output Models

Table of Phase Detector Gains

Linear multiplier:
$K_d = V_{pp}/\pi$, Large phase perturbations ($> \pi/4$)
$K_d = V_{pp}/2$, Small phase perturbations ($< \pi/4$)

Exclusive OR gate, $K_d = (V_{OH} - V_{OL})/\pi$

Digital tri-state output, $K_d = (V_{OH} - V_{OL})/4\pi$

Digital dual output, $K_d = (V_{OH} - V_{OL})/2\pi$

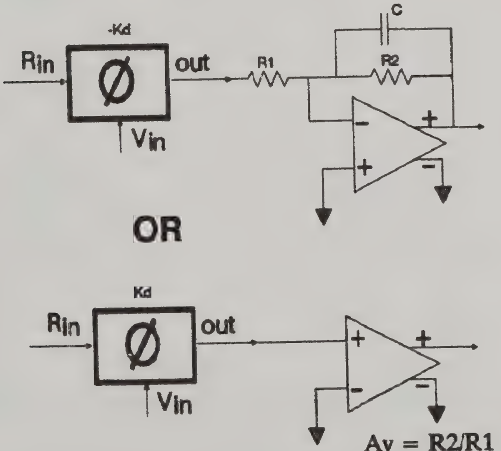
Where, K_d = Phase detector gain in Volts/radian
V_{pp} = Maximum peak to peak output voltage
V_{OH} = Voltage at high logic level
V_{OL} = Voltage at low logic level

Modeling Loop Amplifiers

First, second and third order loop amplifier model examples are given below.

First Order Loop

Notice in the first order loop amplifier of Figure D-9 that the phase detector gain is made negative when using an inverting op-amp type loop amplifier. R1, R2 and C would be the actual components used in the loop circuit. The alternate configuration shown uses an op-amp again as the loop amplifier, but specifies the loop characteristics as part of the op-amp's characteristic gain and bandwidth. Either model will analyze the same, but the second configuration uses fewer nodes.



$$Av = R2/R1$$

$$BW = \frac{Av}{2\pi R2\,C}$$

Figure D-9
Example of 1st Order Loop Amplifier

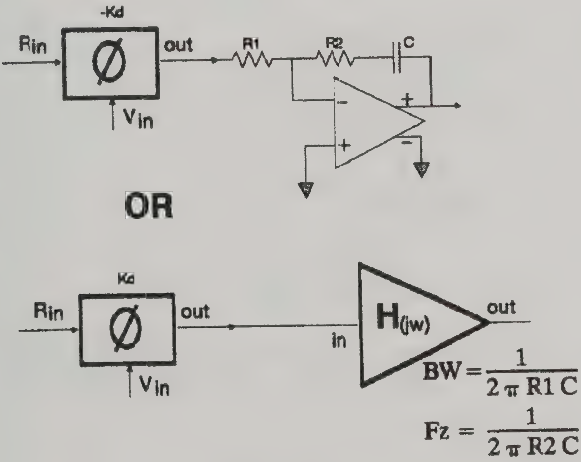
Note that the loop unity gain frequency is less than or equal to:

$$\frac{1}{2\pi R2\,C}$$

for a first order loop.

Second Order Loop

Figure 10 below gives an example of modeling a single ended loop amplifier using either an op-amp or the loop amplifirer element. Again note the negative phase detector gain when using the inverting op-amp



$$BW = \frac{1}{2\pi R1\,C}$$

$$Fz = \frac{1}{2\pi R2\,C}$$

Figure D-10
Example of 2nd Order Single-ended Loop Amplifier

An example of a differential loop amplifier is shown in the previous example of modeling a dual digital output phase detector as Figure D-7 and D-8.

A special case of differential loop amplifier uses the "charge pump" type loop amplifier and is shown in Figure D-11 below.

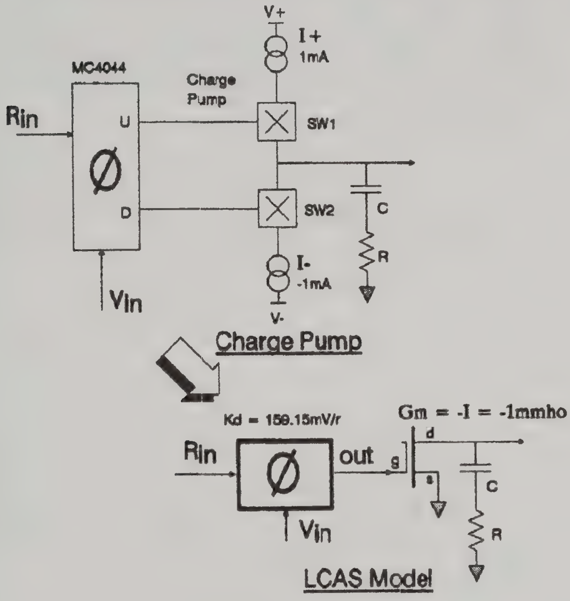

V+
I+
1mA
MC4044
Charge
Pump
Rin
U
Ø
SW1
D
SW2
C
R
I-
-1mA
Vin
V-
Charge Pump
Kd = 159.15mV/r
Gm = -I = -1mmho
d
Rin
Ø
out
g
s
C
Vin
R
LCAS Model

Figure D-11
Model of a Charge Pump Loop Amplifier

For any digital phase detector with a $\pm 2\pi$ (4π) hold range, the Kd is equal to $1/2\pi$ or Kd = 2/Hold range.

Third Order Loop

Third order loop amplifiers are less common than first or second order types. The loop amplifier element was specifically designed to model the more popular second order loop amplifier. Two example configurations for a model of a third order loop amplifier is given in Figure D-12.

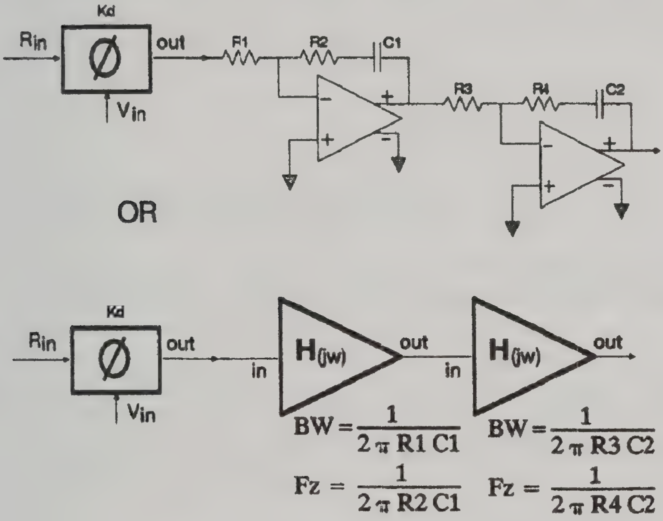

Kd
Rin
Ø
out
Vin
R1
R2
C1
R3
R4
C2
OR
Kd
Rin
Ø
out
Vin
in
H(jw)
out
in
H(jw)
out
$BW = \frac{1}{2\pi R1 C1}$
$Fz = \frac{1}{2\pi R2 C1}$
$BW = \frac{1}{2\pi R3 C2}$
$Fz = \frac{1}{2\pi R4 C2}$

Figure D-12
Model of a 3rd Order Loop Amplifier

Loop Testing

The following examples will demonstrate how to determine the stability, rejection to the phase detectors sampling frequency, noise bandwidth and jitter due to noise and frequency multiplication.

Loop Stability Test Example

Previously in this Appendix was discussed the testing of a PLL for stability. An example circuit is given below which we can analyze for stability as an example.

Assume the circuit of Figure D-13 is a PLL design with a natural frequency, fn of 10kHz. In the form shown if node 1 were the input and node 8 the output the circuit would represent a times 18 multiplier.

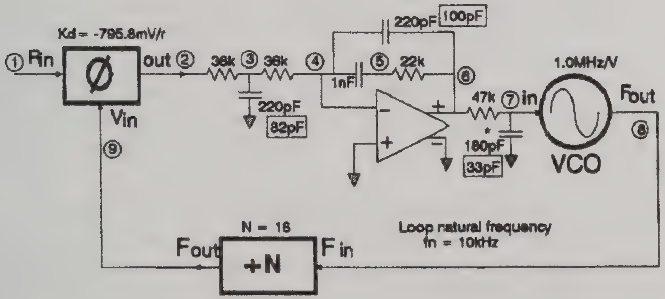

Kd= -795.8mV/r
① Rin
Ø
out ②
Vin
⑨
36k
③
36k
④
220pF
82pF
220pF
100pF
1nF
⑤
22k
⑥
+
−
+
−
47k
⑦ in
*
180pF
33pF
1.0MHz/V
Fout
⑧
VCO
N = 18
Fout
+N
F in
Loop natural frequency
fn = 10kHz

Figure D-13

A circuit file for the sample circuit is included on the master diskette under the file name "LOOPSTAB". The component values not in boxes are those used for the initial design.

To determine if this PLL represents a stable design, we first analyze the circuit over the frequency range of 1.0 to 100.0 kHz. Note the peaking of the response at approximately 10kHz. Will the loop oscillate?

To find out, we ground the phase detectors's VCO input, Vin, (originally node 9) and leave the output node unchanged. Analyze the circuit again and view the graph of the circuit's response. Locate either graphic marker at the point where the phase passes through 180 degrees. Notice that the gain (magnitude) at this point is approximately +2.4 dB, indicating that the circuit will likely be unstable.

Change the capacitor between node 7 and ground at the VCO input to 120pF and analyze the circuit again. Again locate the gain at the frequency where the phase passes through 180 degrees. Now the gain is approximately -2.1 dB, indicating that the circuit is probably stable.

Reconnect the phase detector's VCO input to node 9 and analyze the circuit again. There is still severe peaking near the loop natural frequency, but our previous test indicates that it will not oscillate. Note also that the gain margin is about 2 dB and, that if the VCO gain were to increase by only 28% the loop would become unstable again. Other changes in the circuit's loop gain could lead to instability but the VCO gain is usually the least well controlled element.

As an example of a more stable loop, change the values of the capacitors to those shown on the schematic in boxes, and analyze the circuit once again. The loop is now well behaved and will easily tolerate a VCO gain range from 500 kHz per Volt to 2.0 MHz per Volt.

Spurious Signal Rejection Test

In this example we will determine the ability of a PLL circuit to reject spurious signals. We do this by injecting a signal at the input to the loop amplifier and determining the response vs. frequency for the loop.

For example consider a PLL design for a times 10 multiplier using a 10 kHz reference frequency. Assume that the PLL's bandwidth is required to be 1.0 kHz for close in noise performance and the 10 kHz clock spurs (phase detector clock frequency) are required to be greater than 60 dB down from the carrier at the output.

A digital type phase detector will be used with dual outputs. Therefore a differential loop amplifier is required.

The circuit for this example is shown in Figure D-14. This circuit is also included in the files on the master diskette under the name "LOOPSPUR".

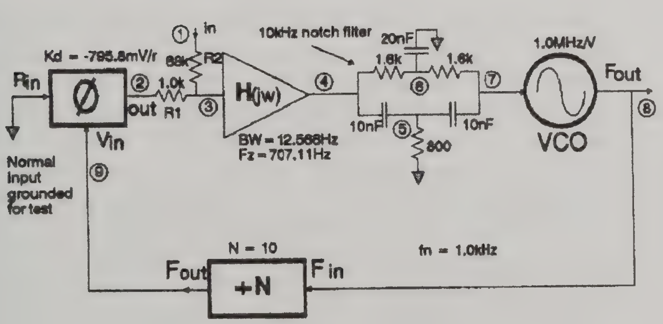

①
in
10kHz notch filter
20nF
1.0MHz/V
Kd = -795.8mV/r
68k
R2
1.6k
1.6k
Rin
Ø
②
1.0k
⑥
⑦
Fout
H(jw)
④
out
R1
③
⑧
10nF
⑤
10nF
800
VCO
Vin
BW = 12.566Hz
Fz = 707.11Hz
Normal input grounded for test
⑨
N = 10
fn = 1.0kHz
Fout
÷N
F in

Figure D-14
Circuit for Spurious Signal Rejection Example

Now lets consider just one of the mechanisms that causes the clocking pulses to propagate through the loop. If each of the phase detector's two outputs produce pulses at the same time and duration, and if the loop amplifier has perfect common mode rejection, there would be no clocking signals beyond the loop amp. However, due to offsets in the op-amp used, the pulses coming out of the phase detector are not of the same duration. Consequently even with perfect common mode rejection in the loop amplifier, there is a difference in the two loop amplifier inputs and this difference is now passed on to the VCO resulting in spurious sidebands.

To make the example more specific, assume that the op-amp has an offset of 10mV. The phase detector in now going to require a small phase error sufficient to match the loop amplifier's 10mV offset. This change in pulse width will produce a small ripple voltage that will be approximately equal to the DC offset times $\sqrt{2}$ Volts RMS in magnitude. If we inject this signal level after the phase detector into the loop amplifier, it will simulate the spurious signal. The resistor divider consisting of R1 and R2 performs the necessary level scaling function. The phase detector's reference input is grounded, thus the only modulating signal in the loop is that introduced into the loop through R2 as shown in Figure D-14.

Now perform an analysis of the circuit with LCAS' output node specified as the VCO output at node 8. Other points in the loop may also be viewed to determine the spurious level. We know that the frequency of the clocking spur is at multiples of 10kHz, starting at 10kHz. While viewing the tabular analysis results use the highlight cursor to locate the frequency nearest 10kHz and observe the magnitude. The voltage column reads approximately 385 μV, meaning a phase modulation of 385 μradians, and the "dB" column reads approximately -68 dB meaning that the total sideband energy at 10kHz is -68 dBc. Since there will be two spurs, one 10kHz above and one 10kHz below the carrier, the energy in each will be approximately -71 dBc. This is depicted in the typical spectrum analyzer display that would be produced by looking at the actual circuit as shown below in Figure D-15.

By changing the analysis frequency range we could cover the higher harmonics of the clock spurs. The level of injection does not change for the higher harmonics because the narrow pulse shape from the phase detector output tends to produce an equal level comb or "picket fence" of frequencies.

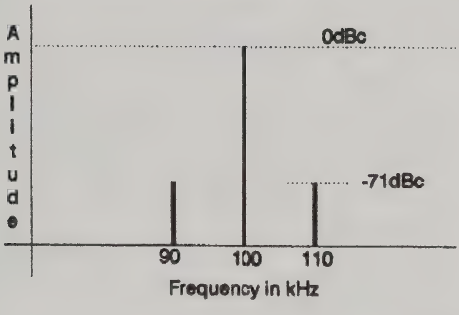


Figure D-15
Spectrum Analyzer Display of Clock Spurs

Note that at 20kHz the sidebands are only about 44 dB down from the carrier. This would normally be improved with additional poles in the loop. At these higher frequencies the added poles generally do not degrade the PLL's response significantly.

Example of Loop Signal Tracking Test

This example shows a basic FM modulator followed by a PLL type demodulator. Two tests will be performed with this circuit:

1. The peak phase error at the phase detector is going to be determined based on both the peak frequency deviation and the frequency of modulation. This will determine if the phase locked loop will be able to track the modulating signal without losing lock.

2. The overall baseband frequency transfer function of the FM modulation and demodulation process using a PLL will be determined.

The PLL circuit for this example is shown in Figure D-16 below. This circuit is included on the master diskette under the name "LOOPTRAK".

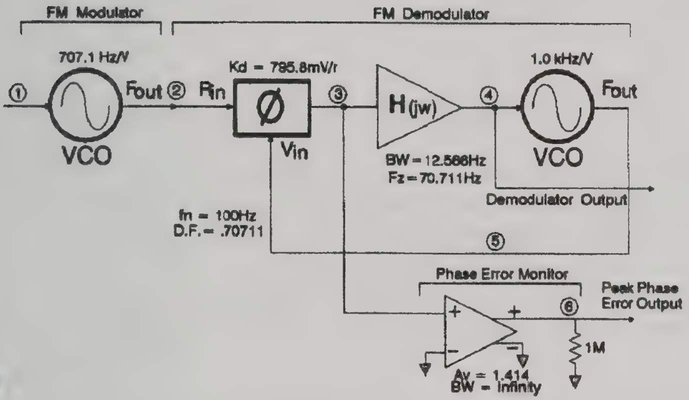

FM Modulator
FM Demodulator
707.1 Hz/V
①
VCO
Fout ②
Rin
Kd = 795.8mV/r
Ø
Vin
③
H(jw)
BW = 12.566Hz
Fz = 70.711Hz
④
1.0 kHz/V
VCO
Fout
Demodulator Output
fn = 100Hz
D.F. = .70711
⑤
Phase Error Monitor
+
+
-
-
⑥
Peak Phase
Error Output
1M
Av = 1.414
BW = Infinity

Figure D-16
Tracking Phase Locked Loop Circuit

Modeling Phase Instead of Frequency Modulation

Note that the modulating VCO can be substituted by a ÷N element if phase modulation is required instead of frequency modulation. If two radians RMS of phase modulation is desired simply specify a ÷N value of 0.5 which multiplies the one radian RMS source by two. Refer to the Divide by N element in Part 3 for more information.

Setting the Peak Deviation

The FM modulator is swept from 1 Hz to 10 kHz as defined by the analysis criteria start and stop frequencies. The peak deviation is 1.0 kHz. This is because the voltage controlling the VCO is a 1.0 Volt RMS signal. The peak value is therefore $\sqrt{2}$ Volts. With a VCO sensitivity of 707.1 Hz/Volt a peak deviation of 1.0 kHz will be acheived. ($707.1 \bullet \sqrt{2} = 1.0$ kHz)

Determination of Peak Phase Error

The output of the phase detector is monitored to determine the phase error at any one deviation level and modulating frequency. Since LCAS always reads values in RMS a scaling factor will be applied to view the peak values. The scaling circuit is the op-amp shown between nodes 3 and 6. To convert the output to peak reading the op-amp is given a gain of $\sqrt{2}$ and a bandwidth of infinity.

The phase detector modeled here is a CMOS digital type with dual outputs and a supply voltage of 5.0 Volts. Therefore if the phase detector's peak output voltage exceeds the supply voltage it will be clipped, and the loop will no longer be closed or locked. ± 5 Volts peak is equivalent to $\pm 2\pi$ radians of peak phase error, which is the maximum phase error limit for this type of phase detector.

With a quick analysis it can be seen that the phase detector's peak output voltage exceeds 5 Volts at frequencies between approximately 73 Hz and 136 Hz. To avoid this condition either the loop bandwidth must be increased, the modulators peak deviation reduced at these frequencies or the frequency of modulation limited to frequencies outside this range.

The peak phase error is the monitored peak phase detector output voltage divided by the phase detector gain. If the phase detector is in Volts per radian then the result is in radians; otherwise the result is in degrees.

Determination of Frequency Transfer Function

By moving LCAS' output node monitor point to the loop amplifier's output on node 4, the overall baseband frequency transfer function can be observed. Any emphasis and de-emphasis filters can be added to the modulator's input and the demodulator's output to represent actual operating conditions. Note that the voltage values shown at the output are again in RMS.

One other point of interest should be noted in the looptrack circuit shown. The 1.0 MΩ resistor placed on the output of the op-amp is not a part of the circuit. It is placed there so that when the output node is moved from node 6 to node 4, there is still at least one other element connected at node 6, a requirement of LCAS.

Example of Jitter Due to Noise and Frequency Multiplication

The following example examines the measurement of jitter in a phase locked loop as the result of both noise and the effect of frequency multiplication.

The circuit chosen for this example is shown in Figure D-17. This circuit is also included on the master diskette under the name"LOOPJTTR".

The PLL used in this example multiplies it's frequency reference by a factor of 500. This frequency multiplication results in both increased phase jitter and noise sidebands as a result of phase jitter.

The energy contained in these sidebands is easily determined in LCAS and therefore allows calculation of the equivalent phase jitter. In most applications the phase jitter is only of concern in a

particular frequency range. For example the phase jitter in voice telephony is commonly measured from 20 to 300 Hz or from 4 to 300 Hz.

In this example we want to create an envelope of the output sideband noise density. We will do this by creating a data file containing the noise density in dB-Hz of the combined noise energy due to the frequency reference feeding the phase detector, and the phase detector noise floor. Then the PLL is analyzed and its transfer function summed with the data file to produce an overall actual sideband noise density.

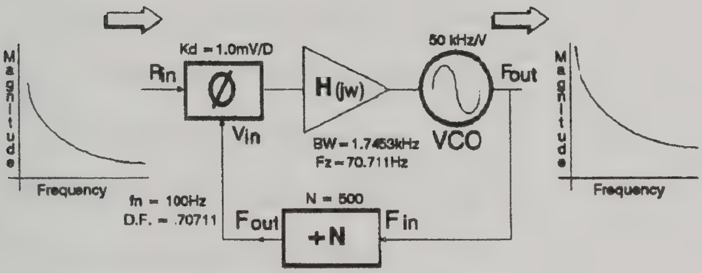

Magnitude
Frequency
Kd = 1.0mV/D
Rin
Ø
Vin
H(jw)
BW = 1.7453kHz
Fz = 70.711Hz
50 kHz/V
VCO
Fout
fn = 100Hz
D.F. = .70711
N = 500
Fout
÷N
Fin
Magnitude
Frequency

Figure D-17

The data file and the PLL analysis must both contain the same frequency range, number of data points and sweep mode.

When the combined graph is displayed the graphic line markers are used to bound the frequency range of interest, and the "A" key (area function) used calculate the energy represented by the magnitude response in this frequency range. After calculation of the sideband noise energy, strike the "J" key and energy values will be replaced by the equivalent phase jitter in both degrees RMS and radians RMS.

Telecommunications links are commonly interested in the peak to peak phase jitter. If the peak to peak value is required then simply multiply the displayed RMS results by 5.15. Telecommunications links are also typically measured for phase jitter in the 4 to 300 Hz and the 20 to 300 Hz ranges.

A data file has been placed on the master LCAS diskette named "R_NOISE.DAT". This file contains a hypothetical noise density spectrum of the sum of a reference oscillator and phase detector. As an example this file can be used in the following sequence of instructions to arrive at a phase jitter measurement of the "LOOPJTTR" circuit.

1. Make a new graph of the data file "R_NOISE" –

/GGDL {Cursor to R_NOISE} [Return] [F6]

If analysis results are present, or

/GDL {Cursor to R_NOISE} [Return] [F6]

If no analysis results are present.

2. Load and analyze the circuit file "LOOPJTTR"
3. Make a new graph of the sum of the two –

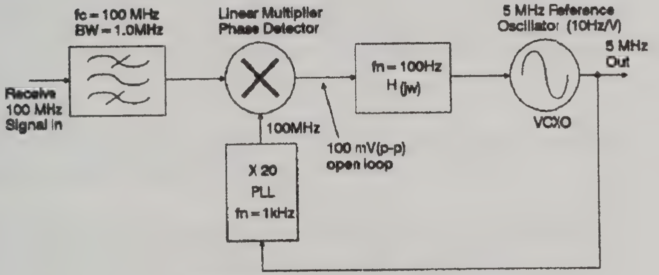
/GNA

4. Place graphic line marker 2 on 20 Hz.
5. Press the "N" key to calculate the total noise power of the magnitude response.
6. Press the "J" key to calculate the jitter represented by this noise value. i.e. from 4 Hz to 300 Hz.
7. Press the "A" key to calculate the noise power from marker 2 to the upper frequency limit.
8. Press the "J" key again to calculate the jitter represented by the noise density from 20 Hz to 300 Hz.

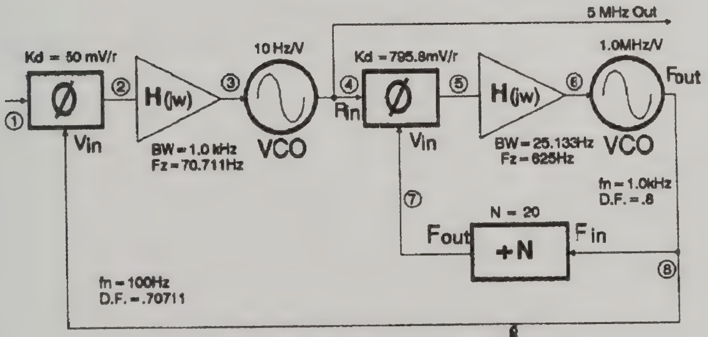
As can be seen, most of the jitter is due to noise close to the carrier, and is due to the reference oscillator. If this were a measurement by a telecommunications jitter meter, the reading would be in peak to peak jitter. To convert the RMS value calculated by LCAS to peak to peak multiply by 5.15.

Example of a Multiple Loop Receiver

Phase locked loop receivers represent a major use of phase locked loop circuits and the multiple loop receiver is a common


fc = 100 MHz
BW = 1.0MHz
Linear Multiplier
Phase Detector
5 MHz Reference
Oscillator (10Hz/V)
5 MHz
Out
Receive
100 MHz
Signal in
fn = 100Hz
H (jw)
VCXO
100MHz
100 mV(p-p)
open loop
X 20
PLL
fn = 1kHz

100 MHz Pilot Receiver Block Diagram


5 MHz Out
Kd = 50 mV/r
10 Hz/V
Kd = 795.8mV/r
1.0MHz/V
①
②
③
④
⑤
⑥
⑦
⑧
Ø
H(jw)
VCO
Vin
BW = 1.0 kHz
Fz = 70.711Hz
Fin
Ø
Vin
H(jw)
VCO
Fout
BW = 25.133Hz
Fz = 625Hz
fn = 1.0kHz
D.F. = .8
N = 20
Fout
÷N
Fin
fn = 100Hz
D.F. = .70711

100 MHz Pilot Receiver LCAS Model

Figure D-18

implementation. The following example will demonstrate how to model a multiple loop receiver within LCAS.

The circuit chosen for this example is a PLL pilot receiver designed to lock onto an incoming pilot signal at 100 MHz and produce a phase locked output of 5 MHz. The pilot receiver is represented by the block diagram in Figure D-18. The second PLL in this circuit is the times 20 multiplier used to regenerate a 100 MHz signal from the 5 MHz output to directly compare with the incoming pilot in a linear multiplier type phase detector.

The LCAS model of this multiple loop receiver is shown in the lower portion of Figure D-18. Node 4 represents the 5 MHz output and node 8 represents the 100 MHz output of the multiplier used to compare to the pilot signal. The input filter of the block diagram is not required for an analysis of the loop performance.

The circuit of this example is included on the master diskette under the name "MULTLOOP".

The circuit is first analyzed with the output node set to node 8. Here the loop characteristics can be verified to determine if the loop appears stable, etc.

Then the output node is set to node 4 to view the recovered 5 MHz signal characteristics.

APPENDIX E

TIPS AND TECHNIQUES

LCAS is an extremely powerful analysis tool. The techniques described below are meant to assist you in simulation and analysis of your circuit designs. Some of the techniques included in this Appendix are:

- A circuit tool for measuring return loss.
- A circuit tool for measuring impedance.
- A technique for scaling output level.
- Modeling and analyzing power supplies.
- Using generated data files.

We would appreciate hearing from users who have discovered other useful ways of making LCAS more versatile.

Measuring Return Loss

The simple circuit shown in Figure E-1, below, can be added, by merging, or direct input during circuit definition, for measuring return loss. This circuit is positioned at the input port to a circuit, so for simplest addition it should be merged before other components. If merged later the node numbers will have to be changed to connect it properly at the input.

To measure the return loss of a circuit, simply make the LCAS circuit criteria "output node" node 3 of this circuit and run the analysis over the desired range.

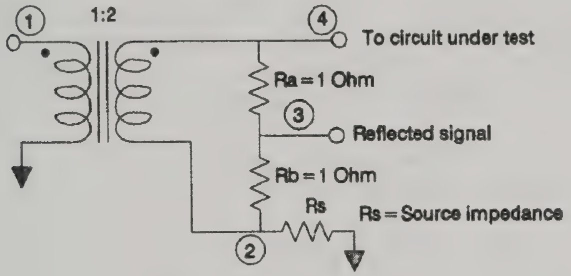


Figure E-1 Return Loss Tool

The circuit must be connected between the LCAS voltage source and the circuit input to operate properly. This circuit operates as follows:

Rs should be set to to equal the impedance of the circuit at the point where it will be connected. For instance a typical IF or RF circuit will have input and output impedances of 50 or 75Ω. To check the return loss at the output of a circuit with a 50Ω impedance, Rs would be set to 50Ω.

The transformer has a 1:2 turns ratio. This transformer connected to the LCAS' zero output impedance 1 Volt RMS voltage source provides a 2 Volt RMS output and isolation from ground. The ideal transformer secondary output is still at zero output impedance. Connection of the source impedance resistor, Rs, between the minus secondary of the transformer and ground causes the plus secondary of the transformer to appear as a single ended 2Volt RMS source with impedance Rs. The two equal resistors Ra and Rb divide the output voltage by two. Ra, Rb and Rs are resistive only, which makes the circuit frequency independant.

If the output of this test circuit is shorted to ground then the full output of the transformer appears across Rs, and one half of the output at node 3. The sign of the output is -180 degrees.

If the output of this test circuit is left open then node 2 is at ground potential due to Rs and the full output of the transformer appears across Ra and Rb, and one half of the output at node 3. The sign of the output is 0 degrees.

If the output of the circuit is connected to a terminating impedance equal to Rs then the voltage across Ra and Rb from nodes 4 to 2 are still at full output but the sign of the signal at node 4 is always 180 degrees from the sign at node 2. This results in the proper zero output at node 3, representing an infinite return loss.

Since the transformer has a turns ratio of 1:2, the 6 dB loss normally encountered with a circuit using both source and termination impedances is no longer present.

Measuring Impedance

The circuit in Figure E-2 can be added to a circuit under test for measurement of circuit impedance at any point within the circuit. This test circuit must be placed at the LCAS voltage source to operate properly. It consists only of 1 FET with a transconductance of -1 mho used to convert the LCAS voltage source to a current source. The output specified in the circuit criteria section for testing using this circuit is taken at the FET drain, node 2.

This test circuit operates as follows:

By assigning the FET a transconductance value of -1 mho the signal at the drain is a current in phase with the gate voltage. The value of the drain current is 1 amp RMS since the gate drive from the LCAS input is 1 Volt RMS.

$$Id = -Gm \bullet Vg$$

$$1.0 = -(-1) \bullet 1$$

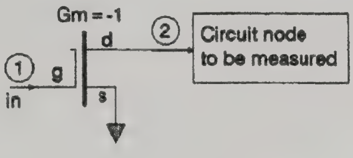


Figure E-2 Impedance Measuring Tool

When this test circuit is connected to a circuit under test, and the LCAS output node set to node 2, every Ohm of input impedance at the connection point results in a voltage of 1 volt at node 2, using Ohm's law, V = IR.

The circuit impedance at the connection point is shown in Volts on the analysis results magnitude listing. For instance the magnitude listing of a tested circuit may list an output of 5.02 kVolts at 1.4 MHz. That means that the circuit impedance at 1.4 MHz is 5.02 kOhms. The phase angle listing directly represents the phase angle of the circuit impedance.

The test circuit should be properly terminated to arrive at correct results using this impedance measuring technique.

Scaling Output Levels

A typical circuit design for filters, amplifiers, attenuators, etc. includes the necessary circuit input and output impedance terminations.

The result of adding the source impedance and output impedance is generally a level at the output 6 dB lower than the circuit under test represents. The graphic display of circuit response normalizes the output level to the peak of the amplitude response, and notes the reference level at the top of the screen. The tabular analysis results however have no built-in facility to scale or normalize the output amplitude.

A very simple circuit addition is shown below in Figure E-3 which can scale the output amplitude to any desired level. This circuit technique also requires no additional nodes and does not affect the circuits response. A FET is added at the circuit input to provide the necessary gain to overcome the termination losses.

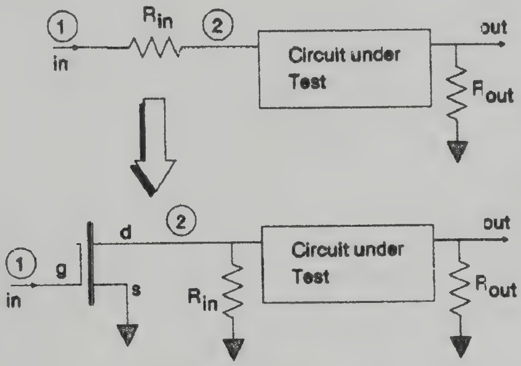


Figure E - 3 Scaling Output

Notice that the addition of the FET to the circuit did not increase the number of nodes required. This makes it simple to add this scaling circuit after a circuit has already been defined without changing any node numbers.

The circuit offers the additional advantage of making the calculation of necessary scaling for unequal source and termination impedances very straightforward.

The transconductance of the FET is set equal to the inverse of the parallel combination of the source and terminating resistance, or

$$Gm = -\frac{Rin + Rout}{Rin \bullet Rout}$$

You may notice that the voltage levels in the circuit under test have doubled by this gain addition at the circuit input, but since there are no power supply rails or other peak limitations, there is no affect on the circuit performance.

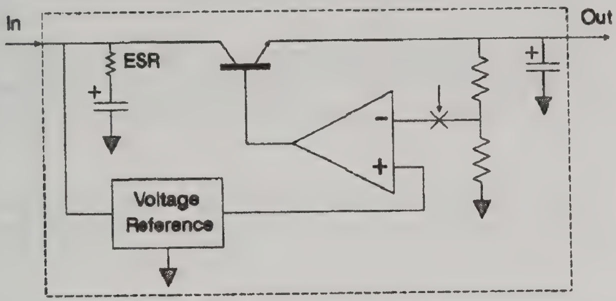
Several of the Example circuits shown in Appendix F use this circuit tool.

Modeling and Analyzing Power Supplies

LCAS does not perform DC analysis of circuits, but is well suited to the analysis of power supply AC performance, which is usually the more critical factor. This section will describe techniques for analysis of power supplies and even show a method of analyzing switching type power supplies.

A basic linear power supply block diagram is shown below.

This circuit assumes that the power supply is fed by a source of DC voltage, usually a transformer and rectifier.


In
Out
ESR
+
+
-
+
Voltage Reference

Basic Linear Power Supply

Figure E-4

If the input is from a rectifier, it has an effective output impedance of Reff which is equal to the transformer output impedance plus the diode on resistance times the diode on to off ratio factor as given in the formula below:

$$R_{eff} = (R_{xfmr} + R_{diode}) \bullet [(T_{on} + T_{off})/T_{on}]$$

Where, T_{on} = Diode forward bias time
T_{off} = Diode reverse bias time

A basic model for analysis of the power supply is shown in Figure E-5 below using the effective rectifier impedance calculated above.

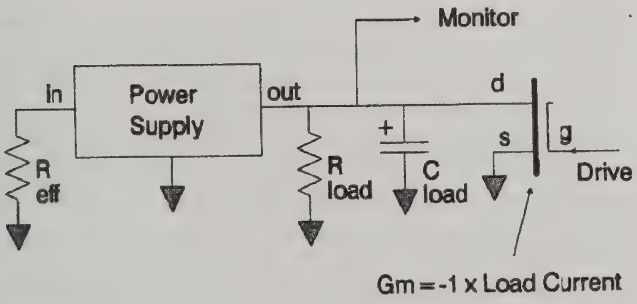

Monitor
In
Power Supply
out
d
+
s
g
R eff
R load
C load
Drive
Gm = -1 x Load Current

Figure E-5

The LCAS source is connected to the drive point and the output connected to the monitor point. The output is a view of the ripple level due to the load current varying at the analysis frequency.

By removing the load R and C and setting the FET's Gm to -1.0, the monitor point reads directly in Ohms and is the output impedance of the power supply.

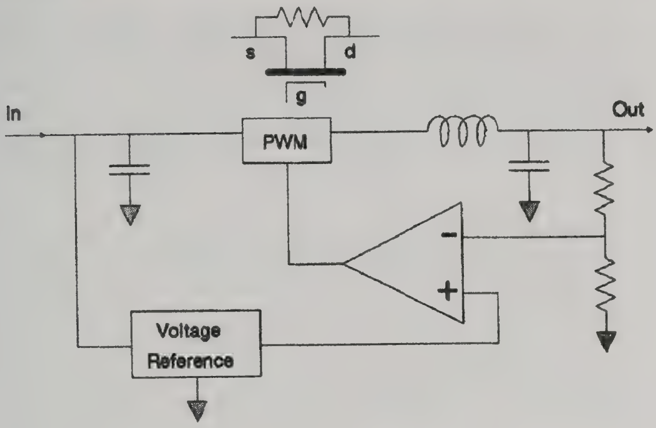
By opening the basic power supplies closed loop at the "X" in Figure E-4, and driving the input to the voltage comparator, the loop characteristics can be observed. By monitoring the voltage that would have been fed back to the comparator, and watching where the phase shift goes through 0° or 360°, the gain indicates if the power supply is likely to oscillate. If the gain is greater than one where the phase is 0° or 360° the supply is likely to oscillate. If the gain is less than one it is unconditionally stable.

Modeling Switching Power Supplies

Although a switching power supply is partly a digital, non-linear device, the feed-back characteristics are usually linear. A model of a swithcing power supply is shown below for use in AC analysis. Notice the similarity to the basic linear power supply shown previously.

In many instances in the analysis of a switching power supply, the pulse width modulator (PWM) section can be replaced by a linear substitute for the analyis of stability and output impedance. The switching frequency of the PWM must be significantly higher than the closed loop analysis range in order to be representative of the circuit. The PWM basically supplies an output current as a function of input voltage, thus serving as a transconductance. The transconductance can be measured by changing the load on the power supply a known amount and measuring the voltage change at the input to the PWM. i.e.:

$$Gm = -\Delta V/\Delta I$$



Basic Switching Power Supply

Figure E-6

A FET serves as a transconductance device as shown in the switching power supply block diagram. The resistance connected between the source and drain is the effective PWM output resistance.

Using Generated Data Files

Several times in this manual the ability to use external data files has been pointed out. Those data files could be generated either by LCAS or externally. Here we will discuss an application of external data files in the determination of signal to noise ratio in a receiver's filters.

Consider a multi-channel communications system where a receiver is required to select one carrier from among many. This common situation is typical of satellite, LOS and broadcast sys-

tems for telephony, video, program and data traffic. Also consider that we desire to determine the effect of a carrier adjacent to that which we are supposed to receive on the signal to noise ratio at the filter which precedes the demodulator. The filter design is partially based on its ability to reject the unwanted carrier, leading to a better signal to noise ratio.

We need three things to determine the composite signal to noise (unwanted signal) ratio in the filter bandwidth. First is a circuit description of the applicable filter(s). Second is a data file or circuit which can generate the transmit spectrum of the desired carrier, and third is a data file or circuit which can represent the transmit spectrum of the unwanted carrier. In many cases the transmit spectrum of the wanted and unwanted carriers are the same, just offset in frequency.

By first analyzing the receiver's filters, and then using the Graph, Data File, Add function to add the desired signals spectrum, one has what remains of the desired signal after the receiver filters.

Next calculate the noise power to arrive at the resulting signal strength. This number will be the "signal" portion of the signal to noise ratio.

Now to determine the noise represented by the unwanted carrier, we again graph the receiver's filter response and add the data file of the adjacent carrier's spectrum. What remains is the amount of the adjacent spectrum leaked into the receiver's passband. By calculating the noise power again, we have determined the "noise" portion of the signal to noise ratio. The ratio of the desired to adjacent signal power is the ratio of the two noise power calculations.

APPENDIX F

EXAMPLE CIRCUIT FILES

Quite a few example circuit files are included on the master diskette for your use in learning LCAS by experimenting, and most important to provide examples of how certain types of circuits are built and modeled in LCAS.

The schematics for several of the included circuit files are given in this chapter along with brief notes describing salient features of the circuit or modeling techniques.

Most of the other circuits provided on the master diskette without a schematic presented here are used as examples in other parts of the manual usually including schematics.

As the contents of the master program diskette are subject to change, the list of circuits given here is not necessarily coincident with that on the master diskette.

The Example Circuit Files on the Master Diskette are:

BP Bandpass filter, Sample circuit used in Part 1 work sessions

XFMR_BP 70 MHz IF "can" filter, schematic in this Appendix

COMB_3 3 section Comb-line filter, Schematic in this Appendix

COMB_7 7 section Comb-line filter

2XTAL_BP 2 crystal bandpass filter, Schematic in this Appendix

6XTAL_BP 6 crystal bandpass filter, Schematic in this Appendix

FWD_TRAN Forward Transversal filter, Schematic in this Appendix

RD_BW Recursive 2 pole Butterworth Transversal Filter

LOOP Example PLL circuit used in Appendix D

1ST_LOOP Example PLL circuit used in Appendix D

2ND_LOOP Example PLL circuit used in Appendix D

3RD_LOOP Example PLL circuit used in Appendix D

LOOPSTAB Example PLL circuit used in Appendix D

LOOPSPUR Example PLL circuit used in Appendix D

LOOPTRAK Example PLL circuit used in Appendix D

MULTLOOP Example PLL circuit used in Appendix D

DELAY Lumped Element 1 mS VF delay line, Schematic in this Appendix

VCXO Voltage controlled crystal oscillator, Schematic in this Appendix

B_REJECT Band reject filter

LM318 Op-Amp model discussed in Part 3

2N2222A Transistor model discussed in Part 3

J310 FET model discussed in Part 3

RF_QUAD RF hybrid quadrature splitter, Schematic in this Appendix

X_OVER Sample circuit used in Part 1 work sessions

XOVR-EX Sample circuit used in Part 1 work sessions

EL_3 3rd order elliptic passive lowpass filter

AT_EL_3 3rd order elliptic active FDNR lowpass filter

AT_EL_LP 3rd order elliptic active Op-Amp lowpass filter, Schematic in this Appendix.

EL_BP_6 6th order elliptic bandpass filter

AT_BW_LP 3rd order active Op-Amp Butterworth lowpass filter

AT_CH_LP 5th order active FET Chebishev lowpass filter

3DB_OCT 3 dB per Octave 20 Hz - 20 kHz filter (pink noise filter), Schematic in this Appendix

P_PREAMP Phono preamplifier, Schematic in this Appendix

QUAD Audio 90 degree splitter.

INPUT_Z Impedance measuring tool discussed in Appendix E

RETLOSS Return loss tool discussed in Appendix E

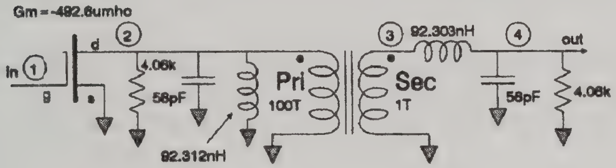
Example Circuit File Schematics

XFMR_BP - IF Filter

This circuit represents the typical IF can type filter found in many superhetrodyne radios. It is a very simple LC filter, but illustrates the use of external inductors to simulate the inductance of the transformer with a prescibed coupling coefficient, k, of .01 and a kQ value of one.

Note that we used the FET scaling tool discussed in Appendix E to remove the level offset in the output due to use of input and outpur terminations. The formulas used to determine the gain required of the FET are also included in Appendix E.

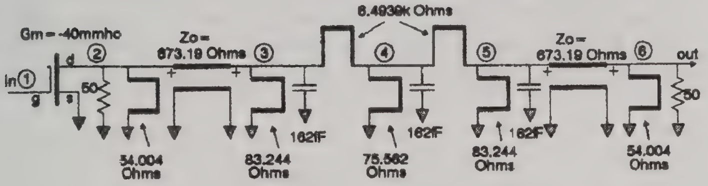
This filter is designed for use at 70.0 MHz as might be found in a communications receiver.



COMB_3 - Comb-line Filter

This is a 3rd order transmission line filter using the transmission line and shorted stub elements as the filter components. The FET scaling tool discussed in Appendix E is used to eliminate offset in output level while using 50 Ohm input and output terminations.

The transmission line and shorted stub elements all have a 1/4 wave frequency of 11.544 GHz.


6.4939k Ohms
Gm = -40mmho
Zo = 673.19 Ohms
Zo = 673.19 Ohms
In ①
d
g
s
②
③
④
⑤
⑥
out
50
50
+
162fF
162fF
162fF
54.004 Ohms
83.244 Ohms
75.562 Ohms
83.244 Ohms
54.004 Ohms

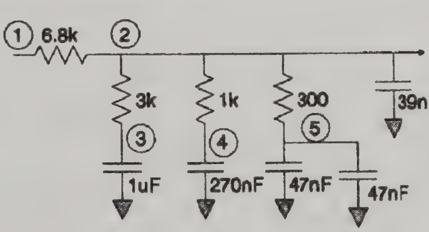
NOTES: 1. All line elements have a 1/4 wave frequency = 11.544 GHz.

The circuit is tuned to provide a 1 dB passband of approximately 7.66 to 7.72 GHz with very well behaved phase and group delay responses.

3DB_OCT - 3 dB per Octave Pink Noise Filter

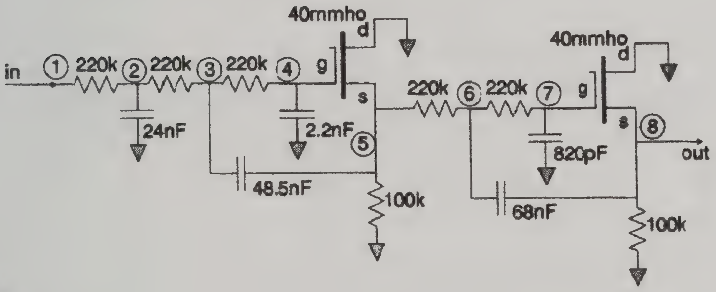
This is a very simple circuit which can filter flat weighted noise accross the audio spetrum at its input and produce pink noise at the output. The circuit weights the noise in equal power per octave from 20 Hz to 20 kHz.

The circuit assumes a low impedance driver and a high impedance input to the next stage.


①
6.8k
②
3k
1k
300
39nF
③
④
⑤
1uF
270nF
47nF
47nF

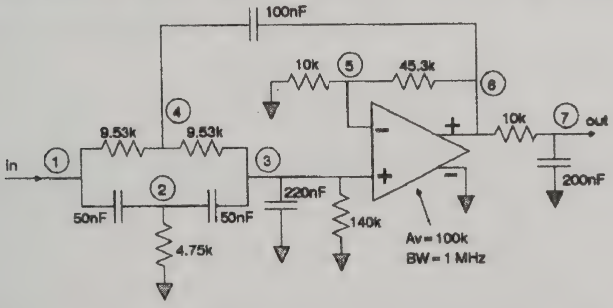
CHEB_LP - Chebishev Low Pass Filter

This is a Chebishev type filter which uses FETs instead of the more common op-amp as the active elements. This filter uses the Salen and Key configuration for a three section followed by a two section low pass filter. The FETS are high gain types.


40mmho
d
g
s
in
①
220k
②
220k
③
220k
④
24nF
2.2nF
⑤
48.5nF
100k
220k
⑥
220k
⑦
820pF
68nF
40mmho
d
g
s
⑧
out
100k

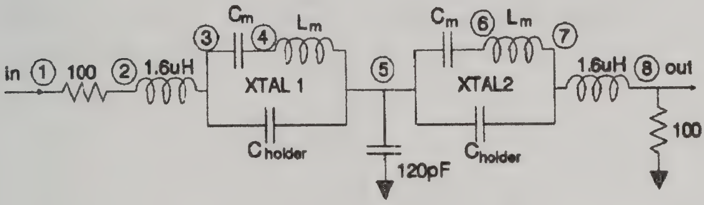
AT_EL_LP - Active Elliptical Low Pass Filter

This is an active low pass filter using an op-amp with feedback to produce an elliptical response. The model is a direct representation of the circuit and could be built as is. The op-amp used is a common type without exceptionally high open loop gain or unity gain bandwidth.


100nF
10k
⑤
45.3k
⑥
④
9.53k
9.53k
10k
⑦
out
in
①
③
②
50nF
50nF
220nF
140k
4.75k
200nF
Av = 100k
BW = 1 MHz

2XTAL_BP - 2 Crystal Bandpass Filter

This is more complex and illustrates the method of modeling a crystal, including its holder, in LCAS. The crystal Q is set by setting the Q of the inductor or capacitor in the circuit labeled Cm or Lm. The bandpass crystal filter has an input and output impedance of 100 Ohms.



XTAL 1 = XTAL 2, Lm = 21.109mH, Cm = 12.00fF, Cholder = 4.0pF
Fc = 10.000MHz, BW = 1.500kHz

This circuit cannot be analyzed without an 8087 co-processor. A data file is provided on the master diskette which can be used to display the graph of the circuit's response. To use the file start LCAS and request a graph of a data file using the command -

/G or /GG

depending on the existance of previous analysis results. The [F6] function key will also work if there are presently no analysis results. At the

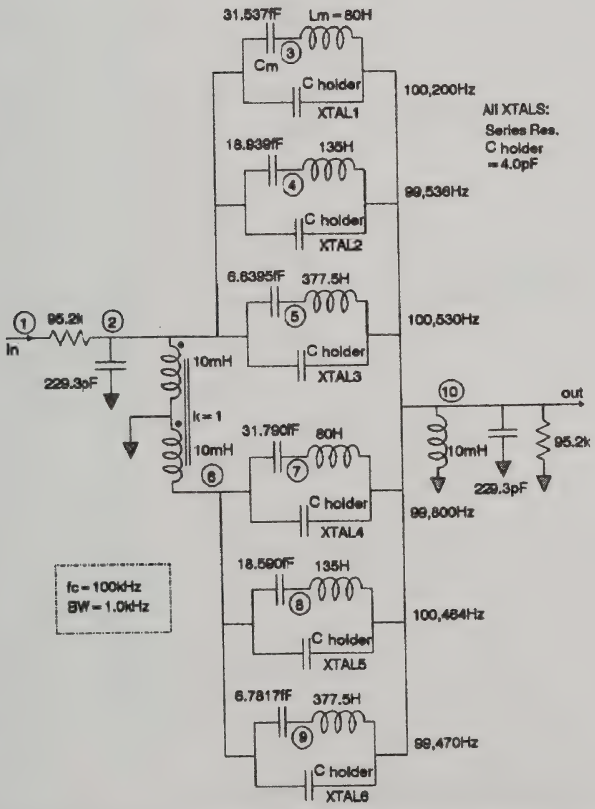
Directory	Load Data File

prompt use "DL" to use the cursor to load from the directory, and select the "2XTAL_BP" file.

6XTAL_BP - 6 Crystal Bandpass Filter

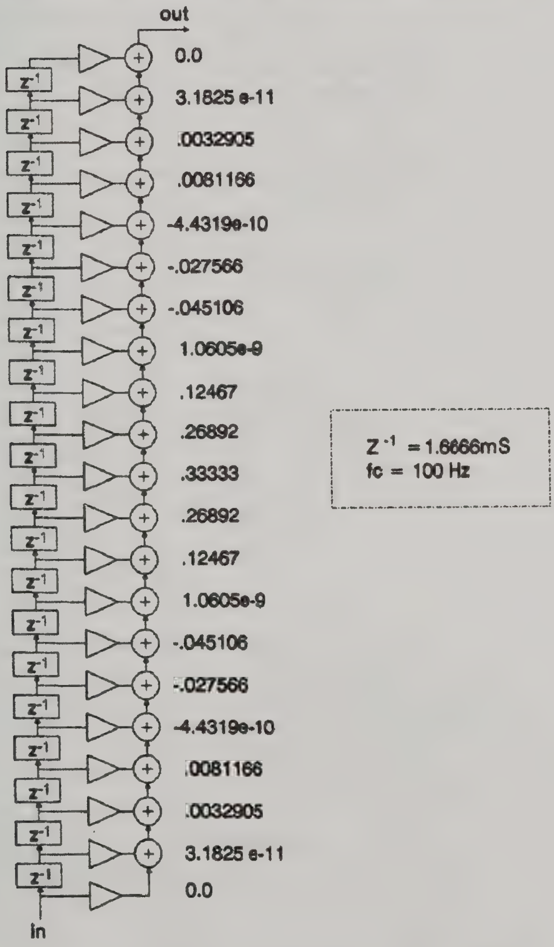
The 6 crystal bandpass filter is a more complex version of the two crystal filter. The same circuit model is used for the crystal and its holder.

This circuit cannot be analyzed without an 8087 co-processor. A data file is provided on the master diskette which can be used to display the graph of the circuits response. Refer to the procedure for the 2XTAL_BP circuit for directions on loading the data file for graphing.


31.537fF
Lm = 80H
③
Cm
C holder
XTAL1
100,200Hz
All XTALS:
Series Res.
C holder
= 4.0pF
18.939fF
135H
④
C holder
XTAL2
99,536Hz
6.6395fF
377.5H
⑤
C holder
XTAL3
100,530Hz
①
95.2k
②
In
229.3pF
10mH
k = 1
10mH
⑥
31.790fF
80H
⑦
C holder
XTAL4
99,800Hz
⑩
out
10mH
229.3pF
95.2k
fc = 100kHz
BW = 1.0kHz
18.590fF
135H
⑧
C holder
XTAL5
100,484Hz
6.7817fF
377.5H
⑨
C holder
XTAL6
99,470Hz

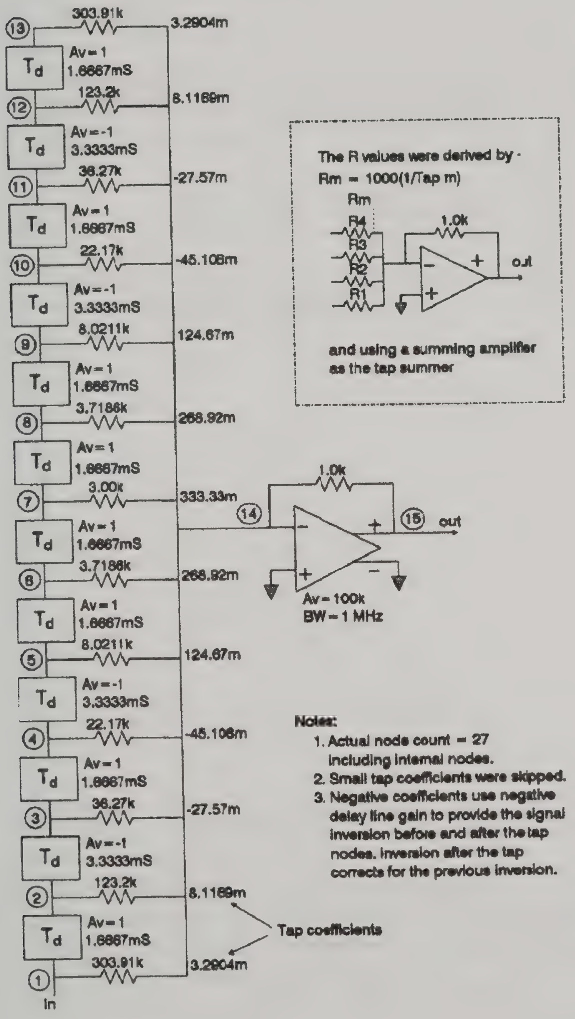
FWD_TRAN - Transversal Filter

This is a non-recursive - or forward - transversal lowpass filter made from delay lines. The original circuit design employs 20 time delays and a summer as shown below. This design could be implemented either digitally or with analog elements.


out
0.0
3.1825 e-11
.0032905
.0081166
-4.4319e-10
-.027566
-.045106
1.0605e-9
.12467
.26892
.33333
.26892
.12467
1.0605e-9
-.045106
-.027566
-4.4319e-10
.0081166
.0032905
3.1825 e-11
0.0
z-1
in
Z-1 = 1.6666mS
fc = 100 Hz

N = 10, hanned tap coefficients, transversal filter

In order to simplify and quicken the analysis process those tap coefficients that were extremely small were simply dropped from the model. The resulting LCAS model of the forward transversal filter is shown below.


13
303.91k
3.2904m
Td
Av=1
1.6667mS
123.2k
12
8.1169m
Td
Av=-1
3.3333mS
38.27k
11
-27.57m
Td
Av=1
1.6667mS
22.17k
10
-45.106m
Td
Av=-1
3.3333mS
8.0211k
9
124.67m
Td
Av=1
1.6667mS
3.7186k
8
268.92m
Td
Av=1
1.6667mS
3.00k
7
333.33m
Td
Av=1
1.6667mS
3.7186k
6
268.92m
Td
Av=1
1.6667mS
8.0211k
5
124.67m
Td
Av=-1
3.3333mS
22.17k
4
-45.106m
Td
Av=1
1.6667mS
38.27k
3
-27.57m
Td
Av=-1
3.3333mS
123.2k
2
8.1169m
Td
Av=1
1.6667mS
303.91k
1
3.2904m
in
Tap coefficients
1.0k
14
15
out
Av=100k
BW=1 MHz
Rm
R4
R3
R2
R1
1.0k
out

The R values were derived by ·
Rm = 1000(1/Tap m)

and using a summing amplifier as the tap summer

Notes:

1. Actual node count = 27 including internal nodes.
2. Small tap coefficients were skipped.
3. Negative coefficients use negative delay line gain to provide the signal inversion before and after the tap nodes. Inversion after the tap corrects for the previous inversion.

This circuit cannot be analyzed without an 8087 co-processor. A data file is provided on the master diskette which can be used to display the graph of the circuit's response. To use the file start LCAS and request a graph of a data file using the command -

```
/G or /GG
```

depending on the existance of previous analysis results. The [F6] function key will also work if there are presently no analysis results. At the

```
Directory    Load Data File
```

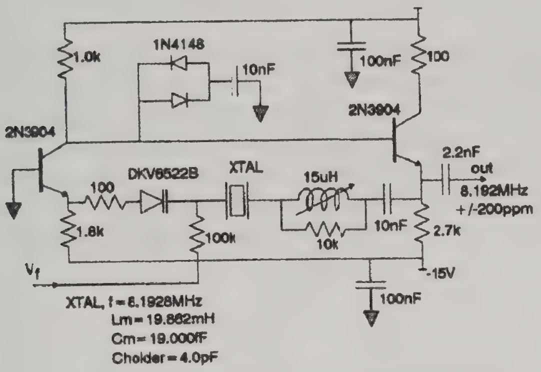
prompt use "DL" to use the cursor to load from the directory, and select the "FWD_TRAN" file.

VCXO - Voltage Controlled Crystal Oscillator

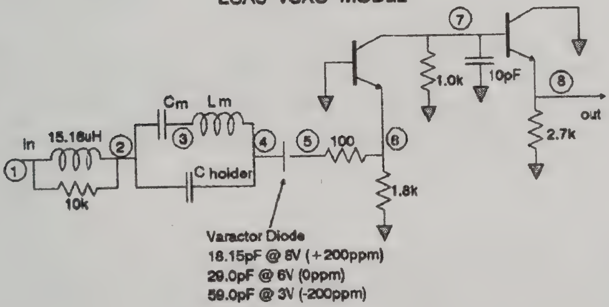
The VCXO circuit is commonly designed as part of a communications receiver which must lock to an incoming signal within a small range of typically +/- 200ppm, while providing a very clean low phase noise output.

Both the actual circuit schematic and the LCAS model are shown to indicate how to model these types of circuits within LCAS.

VCXO CIRCUIT


+15V
1.0k
1N4148
10nF
100nF
100
2N3904
2N3904
2.2nF
out
8.192MHz
+/-200ppm
DKV6522B
XTAL
15uH
100
1.8k
100k
10k
10nF
2.7k
Vf
-15V
100nF
XTAL, f=8.1928MHz
Lm=19.862mH
Cm=19.000fF
Cholder=4.0pF

LCAS VCXO MODEL


7
1.0k
10pF
8
out
2.7k
Cm
Lm
In
15.18uH
1
2
3
4
5
100
6
10k
C holder
1.8k
Varactor Diode
18.15pF @ 8V (+200ppm)
29.0pF @ 6V (0ppm)
59.0pF @ 3V (-200ppm)

The feedback path of the oscillator from the emitter of the right transistor coupling into the crystal circuit is broken in the model, and used as the LCAS input node at 1.

The 10pF capacitor at the base of the right transistor represents the effective capacitance of the 10nF capacitor coupled in series with the junction capacitance of the parallel diodes.

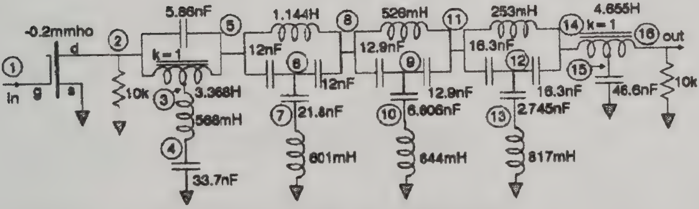
The crystal is modeled as in the crystal filters shown previously. The varactor diode is modeled simply by a capacitor whose value changes to represent the current tuning voltage.

Note that in the actual schematic an output capacitor is shown, but not in the LCAS model. The capacitor serves a DC isolation function in the original circuit and does not effect the analysis. It is not necessary in the model.

When analyzing this circuit set the scale mode to manual, then set the phase' maximum level to zero and leave the minimum unchanged. The analysis is performed three times with each of the varacter diode values shown. The graphs are overlayed, and the frequency of oscillation determined by the point on each phase response where the phase passes through zero degrees, assuming the gain is greater than one.

DELAY - 1 milli-Second Passive Delay Line

This circuit provides a delay of 1 mS over the voice frequency band of 0 to 3.6 kHz. It is built from lumped elements, not just a long piece of wire. This circuit includes an example of the modeling of a tapped inductor with coupling coefficient k=1.


①
in
g
-0.2mmho
d
s
②
10k
5.86nF
⑤
k=1
③
3.366H
568mH
④
33.7nF
1.144H
⑧
12nF
⑥
12nF
⑦
21.8nF
601mH
526mH
⑪
12.9nF
⑨
12.9nF
⑩
6.606nF
644mH
253mH
⑭
16.3nF
⑫
16.3nF
⑬
2.745nF
817mH
4.655H
k=1
⑯
out
⑮
46.6nF
10k

0 to 3.6 kHz Passive, Lumped Element, 1 mS Delay Line

The FET at the circuit's input is used for scaling the output level to eliminate the losses in source and termination impedances.

Refer to Appendix E for more information on the use of this technique.

This circuit cannot be analyzed without an 8087 co-processor. A data file is provided on the master diskette which can be used to display the graph of the circuit's response. To use the file start LCAS and request a graph of a data file using the command -

/G or /GG

depending on the existance of previous analysis results. The {F6} function key will also work if there are presently no analysis results. At the

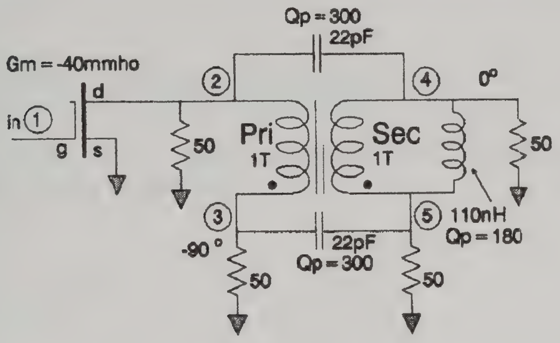
```
Directory    Load Data File
```

prompt use "DL" to use the cursor to load from the directory, and select the "DELAY" file.

After completing the graph of the Delay circuit, press the "D" key to view the group delay, observing the 1.0 mS delay produced.

RF_QUAD - RF Quadrature Splitter

This circuit covers the 52 to 88 MHz frequency range and represents a hybrid splitter. The circuit is bi-directional and has 4 ports. As shown in the schematic below, ports at nodes 3 and 4 are 90 degrees out of phase with each other. The port at node 5 is the internal "waster" load that absorbs any mismatches or canceled signals from nodes 3 and 4. The input scaling circuit can be connected to any port and the output taken at any other port.


Qp = 300
22pF
Gm = -40mmho
②
④
0°
d
in①
g
s
50
Pri
1T
Sec
1T
50
③
⑤
110nH
Qp = 180
-90 °
22pF
Qp = 300
50
50

This hybrid has a 50 Ohm source and termination impedance. All four of the ports are terminated in the circuit.

Notice that the Q of the hybrid device is set by the Q of the two capacitors and the inductor.

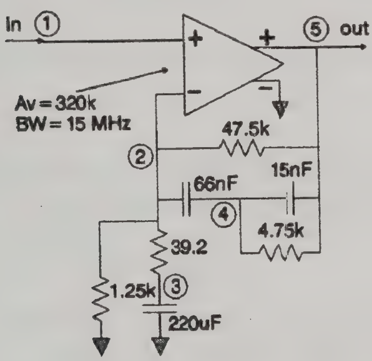
To determine the phase difference from node 3 to 4, first analyze the circuit while monitoring node 3. Then press [F6] to graph the results. Connect the LCAS output to node 4 and analyze again, this time subtracting these analysis results from the previous set by using the graph command -

```
/GNS
```

for Graph, New, Subtract. The resulting graph will now indicate the phase difference between the two output ports.

P_PREAMP - Phono Preamplifier

This is an op-amp type phono preamplifier circuit typical of an LM381 low noise preamplifier.


in ①
+
+
⑤ out
−
−
Av = 320k
BW = 15 MHz
47.5k
②
15nF
66nF
④
4.75k
39.2
1.25k
③
220uF

LM381 type low noise pre-amp

APPENDIX G

DISK FILE CONTENTS

Six types of disk files are written by LCAS:

1. **Circuit Files** – ASCII text defining a circuit and its analysis criteria. Formatted as it appears on the screen without page breaks.
   Extension – .LCA,

2. **Component List Files** – ASCII text listing of a circuits components and analysis criteria. Formatted as it would be sent to a printer.
   Extension – .PRC

3. **Analysis Results Text Files** – ASCII text listing of the analysis results. Formatted as it would be sent to a printer.
   Extension – .PRA

4. **Graphic Bit Map Files** – Binary data image of video screen memory.
   Extension – .PRG

5. **Analysis Results Data Files** – ASCII text list of the analysis results data. Formatted as shown below.
   Extension – .DAT

6. **Fast Fourier Transform Files** – ASCII text data formatted as shown below.
   Extension – .F

The contents and formats of each of these file types is covered below.

1. Circuit Files

The Circuit file is produced when LCAS is given the command -

/FS

or using the [F7] function key. Circuit files are the definition of a circuit by its component types and nodal connections. The LCAS circuit file adds to this the circuit criteria information entered with a circuit before it is saved.

Circuit files are formatted similar to the component screen representation. The difference is that, unlike the component screen, there are no page breaks required in the file. If you use the DOS "TYPE" command to view one of the circuit files, you will see the full form including the double and single line characters used to separate the information into "cells".

2. Component List Text Files

The component text file is produced when LCAS is given the command -

/PTC

The contents of the component list text file are the same as the output produced to go to a printer. That is, the file includes all the information presented in the component screen, but the

double and single line characters used to separate the information into "cells" are replaced by characters which can be printed.

The page breaks and date and time sent to the printer however are not included in this file type.

3. Analysis Results Text Files

The analysis results text file is produced when LCAS is given the command -

/PTA

The contents of the analysis results file are the same as the output produced to go to a printer. That is, the file includes all the information presented in the analysis results screen, but the double and single line characters used to separate the information into "cells" are replaced by characters which can be printed.

The page breaks and date and time sent to the printer however are not included in this file type.

4. Graphic Bit-Map Files

The graphic bit-map file is an image of the video buffer for a color/graphic adaptor card. It contains 16000 bytes corresponding to the 16000 bytes of the video buffer used to create the graph image.

The graphic bit-map file is produced when LCAS is given the command -

/PTG

The contents of the graph file are as follows:

Header -

None

Body -

Byte #1 - First byte of the video buffer.

Byte #2 - Second byte of the video buffer.

Byte #16000 - Last byte of the video buffer.

Notes:

1. The file type is not the same as is used by either basic or any common "paint" type programs.

5. Analysis Results Data Files

The analysis results data file is similar to the analysis results text file except that it is not formatted as a printer file. Instead it is formatted as an array of data usable by LCAS or another program. LCAS uses these data files as inputs which may be graphed, and refers to them simply as "Data Files".

Another program could either generate this type of data file or use one produced by LCAS. An example of the need to produce such a file might be the setting of graphic limits or a "mask" of acceptable values for a certain circuit's response. This type file could be produced manually using a text editor or word processor, possibly beginning with an actual file created by LCAS.

The analysis results data file is produced when LCAS is given the command -

/PDA or /PDG

The data file can be created either from the analysis results in the "present" buffer as viewed in the analysis results listing, or from the data in the "last" buffer as viewed by the last graph produced. These are represented by the two commands above respectively for Print, Data File, Analysis and Print, Data File, Graph

The contents of the analysis results or graph data file are as follows:

Header -

Number of data points (1 to 300), LOG or LIN CR-LF

Body -

Point #1 - Frequency (Hertz), Magnitude (dB), Phase (degrees), Delay (Sec) CR-LF

Point #2 - Frequency (Hertz), Magnitude (dB), Phase (degrees), Delay (Sec) CR-LF

Point #3 - Frequency (Hertz), Magnitude (dB), Phase (degrees), Delay (Sec) CR-LF

Point #N - Frequency (Hertz), Magnitude (dB), Phase (degrees), Delay (Sec) CR-LF EOF

Notes:

1. On the first point and last data points the delay value is always zero.
2. The Delay is optional. It is always generated for output, but not used on input by LCAS.
3. All numbers are ASCII format in scientific notation. e.g. 2.364107e-07.
4. The comma is used as a delimiter between the frequency, magnitude, phase and delay, and the

CR-LF is a carraige return, line feed sequence used between data points.

5. The end of file character, EOF, is appended to the file.

Loading and Saving Data File Information into a Separate BASIC Program.

The following set of routines may be used within a BASIC program to save or load the information in a "Data" file. There are two parts included in the program listing; the first is for loading and the second for saving. These two program parts do not have to be kept together. The line numbers will probably have to be changed to fit into the structure of another program.

```
10 'THE FOLLOWING ROUTINE LOADS A DATA FILE CREATED BY LCAS INTO BASIC
20 '
30 'The array "DAT" contains all the data loaded from the file
40 'DAT(0,0)=The number of data points in the file
50 'DAT(0,1)=The sweep mode, 0=Linear & 1=Log
60 'DAT(N,0)=The frequency in Hertz, DAT(N,1)=The magnitude in dB
70 'DAT(N,2)=The phase in degrees,   DAT(N,3)=The group delay in seconds
80 '
90 '
100 DIM DAT(300,3)
110 INPUT"Data File to Load ";F$
120 OPEN F$+".DAT" FOR INPUT AS 1
130 INPUT#1,DAT(0,0),M$
```

```
140 IF 0< >INSTR(1,M$,"LOG") THEN DAT(0,1)=1
    ELSE DAT(0,1)=0
150 FOR N=1 TO DAT(0,0)
160 INPUT#1,DAT(N,0),DAT(N,1),DAT(N,2),DAT(N,3)
170 NEXT N
180 CLOSE
190 '
200 'THE FOLLOWING ROUTINE SAVES A DATA FILE
    FOR USE BY LCAS
210 '
220 'The array "DAT" contains all the data to save to file
230 'DAT(0,0)=The number of data points in the file
240 'DAT(0,1)=The sweep mode, 0=Linear & 1=Log
250 'DAT(N,0)=The frequency in Hertz, DAT(N,1)=The
    magnitude in dB
260 'DAT(N,2)=The phase in degrees,  DAT(N,3)=The
    group delay in seconds
270 '
280 '
300 INPUT"Data File to Save ";F$
310 OPEN F$+".DAT" FOR OUTPUT AS 1
320 IF DAT(0,1)=0 THEN M$="LIN" ELSE M$="LOG"
330 PRINT#1,STR$(DAT(0,0));",";M$
340 FOR N=1 TO DAT(0,0)
350 WRITE#1,DAT(N,0),DAT(N,1),DAT(N,2),DAT(N,3)
360 NEXT N
370 CLOSE
```

6. Fast Fourier Transform Files

The FFT file is produced when LCAS is given the command -

/PFA   or   /PFG

The FFT file can be created either from the analysis results in the "present" buffer as viewed in the analysis results listing, or from the data in the "last" buffer as viewed by the last graph produced. These are represented by the two commands above respectively for Print, FFT File, Analysis and Print, FFT File, Graph

The contents of the FFT file are as follows:

Header -

Number of FFT points (16 to 2048 in powers of 2),
Frequency step increment (Hertz) CR-LF

Body -

Point #1 - Real part, Imaginary part CR-LF

Point #2 - Real part, Imaginary part CR-LF

Point #(N/2) + 1 - Real part, Imaginary part CR-LF EOF

Notes:

1. The first point is at zero frequency and the last point is the highest analyzed frequency.
2. All numbers are ASCII format in scientific notation. e.g. 3.141593e03.
3. The comma is used as a delimiter between the real and imaginary part and the CR-LF is a carraige return, line feed used between data points.

4. FFT data is represented as a sequence of data points starting at zero frequency, going to the highest frequency, and then a mirror image going back down to the frequency next to zero. The decending sequence negates the imaginary part and is not included in the file since it can be simply calculated. Thus the number of data points is N/2 plus the first zero frequency point.
5. The end of file character, EOF, is appended to the file.

APPENDIX H

INSTALLATION NOTES

This appendix is intended to give a little more information on the installation requirements of the LCAS program and related files to allow users to create their own unique installations if desired. It is not intended to replace the information presented in 'Part 1, Getting Started", on installation procedures.

To summarize, there are very few real restrictions on installation of this program. LCAS is not copy protected and may be placed anywhere there is sufficient room.

The LCAS Master Diskette

The master of the LCAS program is supplied on a standard diskette without any DOS system. The LCAS program is not copy protected for your convenience. A backup master copy can be created by:

1. Directly copying the master diskette to a blank diskette using the DOS DISKCOPY command or,
2. Copying all of the files on the master diskette to a DOS formatted system or data diskette using the DOS COPY command. Note: All the example files may not fit on a DOS "System" diskette.

Requirements for an LCAS Working Copy

A "working copy" is a copy of LCAS for day to day use.

To run the LCAS program requires two files:

LCAS.EXE	The program itself.
LCAS.INT	An initialization configuration file.

LCAS.INT is read by LCAS.EXE during startup and must be on the same diskette and path to be found. If it is not found, LCAS will create one with default values. After startup LCAS is completely resident in memory and requires no further access to the .EXE file. This provides maximum flexibility in placing LCAS and circuit files for operation in your particular hardware environment and according to your desires.

The only time LCAS requires access to the LCAS.INT file after startup is if the configuration is changed by using the Setup command and the Update option is chosen. LCAS will then write a new copy of the file LCAS.INT to disk in the disk and path current when LCAS was started. LCAS should therefore not be started using a path command because any new configuration file will be written into the disk/path from which LCAS was called. Instead LCAS should always be started by first changing the directory path to that where LCAS.EXE resides.

For example consider a system where LCAS.EXE and LCAS.INT are in a hard disk directory as generated by the "INSTHARD" batch file supplied on the master diskette. LCAS is then in the directory C:\DATUM and a batch file is required to start LCAS from the root directory. The proper batch file contents would be:

```
CD \DATUM
LCAS
CD \
```

The purpose of the final "CD\" is to return to the root directory after LCAS is quit.

Creating a Working Copy of LCAS

To create a working copy of LCAS you would simply place the LCAS program and the desired sample files onto a DOS formatted system diskette, or onto your hard disk. Circuit files can be placed either with the program or on a separate diskette or directory.

If there is room on the diskette it does not matter what other files it contains. For instance you may have multiple programs that you use to design circuits. There is no reason that they could not all be placed on a 1.2 Mega-byte diskette used on an "AT" type computer.

Hard Disk Users:

You have a choice of placing your circuit files either on the hard disk in the same or different directory than LCAS, or on a separate floppy diskette. Each circuit file is normally 1 to 10k in length.

Use of Path Names in the Set-Up

The setup option within LCAS allows you to specify a separate drive and path for each of the four file types allowed; Circuit, Text, Data and FFT. DOS allows you to specify a path in several modes and it can be slightly confusing.

For instance, when the standard hard disk installation is used, all files are in a directory with a full path designation of

"C:\DATUM\LCAS". LCAS is however already in the "C:\DATUM" directory. To specify the path to reach the files from, the full path name of "C:\DATUM\LCAS" could be used but is not required since the LCAS program is running from within the "C:\DATUM" directory. The path "\DATUM\LCAS" or just "LCAS" could also be used. Note however that the path "\LCAS" could not be used because the initial "\" means start at the root directory.

Configuration

You now have a working copy of your LCAS diskette. The configuration of this diskette for your computer hardware is covered in Part 1 of the manual. The default configuration used by LCAS will work on any computer hardware setup.

APPENDIX I

ERROR MESSAGES

1. ERROR MESSAGES IN ALPHABETICAL ORDER

± ∞ in Analysis Results – When LCAS has an underflow or overflow during calculation of the analysis results at the present frequency point, it will place the plus and minus infinity sign in the respective position and continue with the analysis. Refer to the problem locator in Appendix J for a discussion of possible solutiions.

BAD ENTRY !!! You tried to make an illegal entry. Either the input and/or output node(s) was not specified or does not refer to nodes currently in the circuit. The start and/or stop frequency was improperly specified, ie the stop frequency is lower than the start frequency. The number of data points and/or sweep information was not specified. A character specified for the printer setup string is out of range. Or a file name entry contains more than 8 characters excluding the drive designator.

CAN'T BACK UP !!! This only appears in graphing data with manual scale mode set if you attempt to escape from graphing the data. The data has already been manipulated by a requested function and the original cannot be retrieved. You must continue to graph the data.

CAN NOT EXPAND ANYMORE !!! You tried to expand a circuit beyond the frequency resolution, 8 digits, of this program.

CAN'T INTERPOLATE DATA, UNDERFLOW/OVERFLOW ERROR !!! In an attempt to calculate the data for an FFT file an intermediate value exceeded the dynamic range of the computer.

CAN'T CALCULATE NOISE POWER, UNDERFLOW/OVERFLOW ERROR !!! In an attempt to calculate the noise power an intermediate value exceeded the dynamic range of the computer.

COMPONENT LIST FULL !!! You tried to input more than 128 components in LCAS (or more than 12 components in the demo program "DLCAS"). Reduce the number of components or analyze the circuit in sections and sum them graphically.

CONFIGURATION FILE LCAS.INT NOT FOUND OR INCORRECTLY FORMATTED !!! CREATING DEFAULT LCAS.INT FILE NOW During entry to the program, the configuration file "LCAS.INT" was not found or was incorrectly formatted. The program will attempt to generate a new file that assumes the current default drive and path, no 8087, a null print string, and printer port #1 (LPT1:). This file will need to be updated based on the particular configuration you have after successful entry to the program.

DISK ERROR !!! Either the disk drive has developed a fault or the diskette is defective. Repair defective drive and/or replace bad diskette.

DISK FULL !!! All diskette storage space on the current drive is in use. If there are any files on the diskette that you no longer need, erase them; or, replace the diskette with one that has sufficient space left on it. Then retry the operation.

DISK NOT READY !!! The diskette drive door is open, there is no diskette in the drive or an improperly formatted diskette is in the drive. Place the correct diskette in the current drive and close the door.

DISK WRITE PROTECTED !!! You tried to write to a diskette that is write protected. Make sure you are using the correct dis-

kette. If so, remove the write protection, then retry the operation.

ERROR !!! An undefinable error has occurred. Try rerunning the program. If the error still occurs please note the conditions surrounding the error and inform us of the problem.

FILE ALREADY EXISTS ? You tried to save a file to diskette with the same name as an already existing file on that diskette. Either type "Y" to replace the file on the diskette or type "N" to return to the file name prompt to save the file with a new name.

FILE INCORRECTLY FORMATTED !!! You tried to load a circuit or data file that is incorrectly formatted for input to this program. Check the file name for correctness. Note, files generated by LCAS may not be compatible, with DLCAS, the demonstration version of LCAS, due to limitations in the number of nodes, number of components and types of components supported by DLCAS.

FILE NOT FOUND !!! You tried to load a file that does not exist on the diskette in the current drive. Check file name, diskette and current drive designation for correctness.

INSUFFICIENT DATA TO GRAPH !!! To graph data properly a minimum of three data points is required. Change the number of data points to 3 or more, reanalyze the circuit and then retry the graph operation.

INSUFFICIENT DATA TO PRINT !!! To print data properly a minimum of three data points is required. Change the number of data points to 3 or more, reanalyze the circuit and then retry the print operation.

NO ANALYSIS RESULTS TO DISPLAY !!! There is currently no analysis results to view. Analyze a circuit and retry the operation.

NO ANALYSIS RESULTS TO PRINT !!! There is currently no analysis results to print. Analyze a circuit and retry the operation.

NO CIRCUIT TO ANALYZE !!! There are no components in the component list to analyze. Enter components and retry the operation.

NO CIRCUIT TO NAME !!! There are no components in the component list when the circuit name function was requested. Enter components and retry the operation.

NO CIRCUIT TO PRINT !!! There are no components in the component list to print. Enter components and retry the operation.

NO CIRCUIT TO SAVE !!! There are no components in the component list to save. Enter components and retry the operation.

NO COMPONENTS TO MERGE !!! There are no components in the component list to merge to. In order to merge circuits there must be something to merge to. Enter components and retry the operation.

NO FILES FOUND !!! You did a directory and the diskette in the current drive has no circuit files on it. Circuit files are those with the file extension ".LCA". Or you did a directory of data files and the diskette has no data files on it. Data files are those with the extension ".DAT". Either of the above could fail if the path specified in the "Set-up, Default Drive" command does not follow DOS conventions.

NO GRAPH TO DISPLAY !!! There is currently no graph to view. Analyze a circuit or load a data file and graph it.

NO GRAPH TO PRINT !!! There is currently no graph to print. Analyze a circuit, graph it and retry the operation.

NO GRAPHICS ADAPTER !!! Your computer is not equipped with either a standard or an enhanced color graphics adapter and you tried to do a graphic type function. Install a color graphics adapter and retry the operation.

NODE ## SKIPPED !!! The node indicated was skipped. Nodes must be consecutive numbered, ie 1,2,3,4... not 1,2,4,5... Return to component screen and edit nodes to conform to this requirement.

NODE ## USED ONLY ONCE !!! The node indicated was used only once. Nodes cannot be left floating. All nodes must be terminated in some manner, returning ultimately to ground. Note however, some circuit components are constructed from a number of more basic components. This allows nodes on selected components to be left floating without being flagged or causing a problem.

OUT OF MEMORY, 640K MINIMUM !!! This program requires a minimum of 640k of free memory. Remove any resident programs such as SideKick, Backscroll or a ram disk, etc and reboot the system. If your computer is equipped with less than 640k of memory then it will require additional hardware to bring it up to this level. This error will only occur while entering the program.

PATH NOT FOUND !!! An incorrect path was specified in the "Set-Up, Default Drive" command.

PRINTER ERROR !!! You tried to print to the specified printer port, LPT1:, LPT2: or LPT3: and the printer failed to respond. Make sure the printer port is specified correctly, the printer is connected to the proper printer port LPTx:, the power is on, the printer has paper and the printer is on line. Then retry the operation.

REPLACE FILE (Y/N) You tried to save a file to diskette with the same name as an already existing file on that diskette. Either type "Y" to replace the file on the diskette or type "N" to return to the file name prompt to save the file with a new name.

STRING TO LONG !!! You tried to enter more than 270 characters for the printer setup string. No more than 270 characters maybe entered for the printer setup string.

TO MANY COMPONENTS !!! Some components are constructed of many more basic components. Therefore, during analysis there maybe many more components than those directly specified. The maximum number of components that can be analyzed internally is 512. Reduce the number of components used.

TO MANY NODES !!! Some components are constructed of many more basic components. Therefore, during analysis there maybe many more nodes than those directly specified. The maximum number of nodes that can be analyzed internally is 64. Reduce the number of nodes used. Ground is considered one node.

UNRECOVERABLE DISK ERROR !!! A fault occurred while trying to load the default configuration file that was not recoverable. The fault may of occurred because the disk drive was not ready, the diskette was full, the diskette was write protected, the disk drive is broken or the diskette is defective.

UNRECOVERABLE SYSTEM ERROR !!! A fault occurred while trying to load and/or configure this program. Try rebooting your computer and reloading the program. If the error persists, run the diagnostic program supplied with your computer. If no problems can be found then the diskette supplied with LCAS maybe defective. Return the original diskette for replacement.

WARNING CO-PROCESSOR NOT FOUND !!! You requested operation with an 8087/80287 and one is not installed. Either install the co-processor or configure LCAS for no 8087.

2. ERROR MESSAGES BY TYPE

DISK ERRORS

DISK ERROR !!!
DISK NOT READY !!!
DISK WRITE PROTECTED !!!
DISK FULL !!!
FILE ALREADY EXISTS ? REPLACE FILE (Y/N)
FILE INCORRECTLY FORMATTED !!!
FILE NOT FOUND !!!
NO FILES FOUND !!!
NO CIRCUIT TO SAVE !!!

PRINTER ERRORS

PRINTER ERROR !!!
STRING TO LONG !!!
NO ANALYSIS RESULTS TO PRINT !!!
NO CIRCUIT TO PRINT !!!
NO GRAPH TO PRINT !!!

ANALYSIS ERRORS

± ∞
NO CIRCUIT TO ANALYZE !!!
NO ANALYSIS RESULTS TO DISPLAY !!!
CANNOT EXPAND ANYMORE !!!

GRAPHICS ERRORS

NO GRAPHICS ADAPTER !!!
NO GRAPH TO DISPLAY !!!
INSUFFICIENT DATA TO GRAPH !!!

CIRCUIT ERRORS

COMPONENT LIST FULL !!!
TO MANY COMPONENTS !!!
TO MANY NODES !!!
NODE SKIPPED !!!
NODE USED ONLY ONCE !!!
NO COMPONENTS TO MERGE !!!

MISC ERRORS

BAD ENTRY !!!
CAN'T CALCULATE NOISE POWER, UNDERFLOW/OVERFLOW ERROR !!!
ERROR !!!

APPENDIX J

PROBLEM LOCATOR

LCAS is designed to be as error free as possible. This section is intended to help the user through any known problems in implementation of circuits withing LCAS. User input can help to eliminate or explain additional problems in the future.

Known problems are discussed below with possible solutions:

1. Editing Problems -

Cursor Control (Arrow) Keys do not perform as expected

The **[Num Lock]**, Number lock key may be set to produce numbers instead of cursor functions. Try pressing the **[Num Lock]** key once to toggle the numbers mode off.

Copying Components Yields Nodal Number Errors

The components is the range copied from had nodal numbers which were discontinuous. In some cases this can lead to errors in computing the new node numbers. The solution is to be very careful when originally specifying node numbers.

Renumbering Components Yields Nodal Number Errors

The only known problem here is shown in an example in Part 1, Example session two. When a negative renumbering increment is given with low node numbers, nodes may end up being tied to ground.

2. Analysis Problems -

Infinity Signs in Analysis Results.

This is very rare when using the 8087 NDP so it is assumed that one is not present. If one is present, then the circuit probably has a description error, most likely in the node numbers.

The software calculations use standard double precision routines which can handle numbers of approximately 10 to the plus or minus 37th power. This may seem large (and small) but linear matrix calculations can overflow or underflow. Rather than aborting the program, LCAS will show an overflow or underflow as an infinity sign and go on to the next step.

The obvious solution is to utilize the 8087. Another possible solution is to normalize all the component values for another frequency range. Points very close to DC (as in microhertz), or at extremely high frequencies (for instance at greater than 10 GHz) could also contribute to the problem. Unfortunately is is impossible to describe a method to scale component values for another frequency range as this is a function of the circuit design.

The order of the nodes used in the calculations may be a determining factor in the value of intermediate results which can over- or under-flow. For some circuits, simply renumbering the nodes may eliminate the problem. It is a good idea though to keep the input node the lowest number and the output node the highest number.

3. Graphing Problems -

Graph won't print on Printer

The most likely cause of this is that your printer does not use the Epson standard graphics commands. If this is the case, the only solution is to use a "grab" program as supplied with some "paint" programs, to grab the graphic screen and print separately.

If your printer does use the Epson graphics commands then check the port used and connections. Are you able to print graphics from other programs?

Graph won't print on Screen

The graphics routines in LCAS require a color/graphics or EGA adaptor to work. LCAS does not have to be configured for the graphic adaptor as it determines the presense of one itself.

LCAS does not work with "monochrome graphics" adaptors. There are programs available which allow a "monochrome graphics" adaptor to simulate a color/graphics adaptor. LCAS has not been tested with any of these programs.

If you have a graphics adaptor and can't get an output, make sure that your adaptor does not require a special setup or configuration program before it will work.

4. File Problems -

File(s) Not Found

The most common file problem is that a file or a type of file cannot be found. Check the "Set-Up" configuration for the four different file types to verify the correct drive and path settings. See the notes in the Installation of Appendix H.

APPENDIX K

GLOSSARY

Analysis Criteria A description of the criteria for analyzing a circuit within LCAS. Includes the start and stop frequencies, number of data points, frequency increment mode and the circuit's input and output nodes.

Analysis Results Screen One of three screen in LCAS. Used to display the results of a circuit analysis and also the analysis criteria. Can be changed to by pressing the **[F2]** function key after an analysis is completed.

CGA Color Graphics Adaptor. A monitor driver for the PC that allows display of both text and graphic information.

Circuit File A disk file containing the description of a circuit including the list of components, component parameters, nodal connections and circuit analysis criteria.

Component Screen One of three screen in LCAS. Used to display the component listing and connections plus the analysis criteria. The component screen is used to enter and edit circuit information. Can be changed to by pressing the [F1] function key.

Co-processor An adjunct to the micro-processor used in the computer. The most common type is called a Numeric Data Processor which handles mathematical functions for the main processor when requested by the program. LCAS can use a Numeric Data Processor and will speed up mathematical calculations by a factor greater than 7.

Cursor An on screen indicator of present input location. The cursor can take several forms in LCAS, either character or cell sized for text or numerical entry, or as dashed line markers on the graphic screen.

Cursor Keys The keyboard set of keys with the four arrows designed to move the on screen cursor. Usually grouped around the numeric keypad.

DOS Disk Operating System. The standard underlying executive from which most other programs are run. Either PC-DOS or MS-DOS 2.0 or later must be operating before LCAS is invoked.

Data File A disk file containing numerical data describing a frequency transfer function. The most common form is a data listing of the LCAS analysis results.

Default The values chosen for optional parameters before or unless set by the user. These may be in DOS or in LCAS.

Directory 1. That section of a disk containing a group of files under one name. Usually this refers to hard disk directories. 2. The listing of files on the screen as when using the DOS "DIR" command or the LCAS "/FD" command.

Dielectric constant The measure of the permittivity of an insulating substance. The common dielectric constant is a dimensionless ratio of the permittivity of the substance to that of free space. The relative dielectric constant of an insulator in a capacitor is the ratio by which the capacitance is increased when the dielectric material replaces a vacuum between the capacitors electrode plates.

Drive A common term for one type of the mass storage device used in computers. Refers to a floppy or hard disk drive. Drives are named and referred to by DOS by their designated letter followed by a colon, beginning with A:, B:, etc. The C: drive is normally the computer's hard disk.

EGA **Enhanced Graphic Adaptor.** A CRT monitor driver board for the PC with higher possible resolution than the standard Color Graphics Adaptor.

Engineering Notation A numeric representation wherein a number is shown as a mantissa between 0 and 999 and its exponent. The exponent increments in 3s corresponding to the engineering multipliers (Kilo-, Mega-, Giga-, etc).

FFT File A disk file which can be generated by LCAS. The file contains frequency transfer function information in rectangular coordinate format refering to a Fast Fourier Transform. This file type is intended for use with separate Fast Fourier Transform programs.

File A collection of data usually contained on a floppy or hard disk. Files are used by LCAS to store circuit information and analysis results.

Function Keys The group of keys on the left or above the main letter keys on the keyboard with the "F" label, for function. They range from F1 thru F10 or F12 depending on the type keyboard.

Graph Screen One of three screen in LCAS. Used to display analysis results or data file information in graphic format. Can be changed to by pressing the [F3] function key after a graph is completed.

Linear Circuit Analysis The computation of a linear circuits frequency transfer function (magnitude and phase characteristics as a function of frequency). LCAS performs an analysis of the complex coefficients of multiple simultaneous equations. The equations represent the admittances of components connected to each node

Microstrip In electronics a microstrip is a form of transmission line built onto a physical structure. The microstrip consists of a strip of conductor above a ground plane, separated by a dielectric material. It is often a copper trace on a printed circuit board with well controlled characteristics at the intended frequency of use.

Node A connection point in a circuit where two or more components are connected together. Represented in LCAS by a unique number.

Parallel Interface A connection from the PC to a Parallel device. The common parallel devices in use are most printers, and some plotters. DOS names parallel interfaces LPT1:, LPT2:, etc.

Path The routing thru the disk file directories to a given subdirectory or file.

PCB or Printed Circuit Board The composite board on which a circuit is finally built. LCAS can simulate some of the circuit board parameters for traces used as transmission lines.

Q Factor or Figure of Merit A representation of the quality or figure of merit of a component. The Q of a component is equivalent to 1/dissipation factor.

Scientific Notation A numeric representation wherein a number is shown as a mantissa between 0 and 1 and its exponent.

Serial Interface A connection from the PC to a serial device. The common serial devices in use are daisy wheel printers, mice and modems. The common serial interface adheres to a standard known as RS-232. DOS names serial interfaces COM1:, COM2:, etc.

Text File A disk file containing information in a form that could be sent directly to a printer. Information in the text file is separated into "cells" as it appears on the video screen with line charaters replaced by ascii dashes, equal signs and "|" symbols. Text files can be either "circuit" or "analysis results". Graphic bit-map files are also referred to as text files.

Transversal Filter A class of filter that is based on delay elements as the only frequency dependant components.

APPENDIX X

USER SUPPORT PLAN

DATUM Systems has attempted to keep the cost of LCAS very low. We hope this will encourage the use and spread of LCAS, but does not leave much money for advertising. We also have not used copy protection for your convenience. That is why a copy of the demonstration program is included with the purchase of this program. Please feel free to give copies of the demonstration program to others who may be interested in LCAS.

DATUM Systems offers the following incentives to *registered* purchasers of LCAS:

1. Low cost updates to future versions of the program. Registered users will receive information on updates and related new programs via mail.
2. High quality documentation.
3. Technical assistance on operation of the LCAS program at our office number, 10:00AM to 5:00PM PST, Monday to Friday. Sorry, we cannot help you design circuits though.

   The Phone Number for technical assistance is:

   (408) 988-0858

Registration

If this program was purchased directly from DATUM Systems then you are already registered, but please fill in and mail the registration form as confirmation. If the program was purchased

from a vendor or third party, you should fill in and mail the User Registration Card in the rear of this manual to receive information on future updates. If no card is present, mail your name, address and the serial number of your copy of the program to DATUM Systems. The serial number is displayed when you "Quit" LCAS, but before confirming with "Y".

If you move and wish to still receive information on updates, either write or call to notify us of your new address.

Corporate and Multi-Copy Users

Datum Systems also offers the same incentives to corporate and other multi-copy users of LCAS. Purchasers of multiple copies of LCAS will also receive a discount on the schedule below for purchases made on one order at one time only. That is:

10% discount at 5 to 9 copies

15% discount at 10 to 19 copies

20% discount at 20 copies or more

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